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MICROWAVE ASSOCIATES INC BURLINGTON MA

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KA-BAND MICROWAVE INTEGRATED CIRCUIT SPDT SWITCH DEVELOPMENT. (U)

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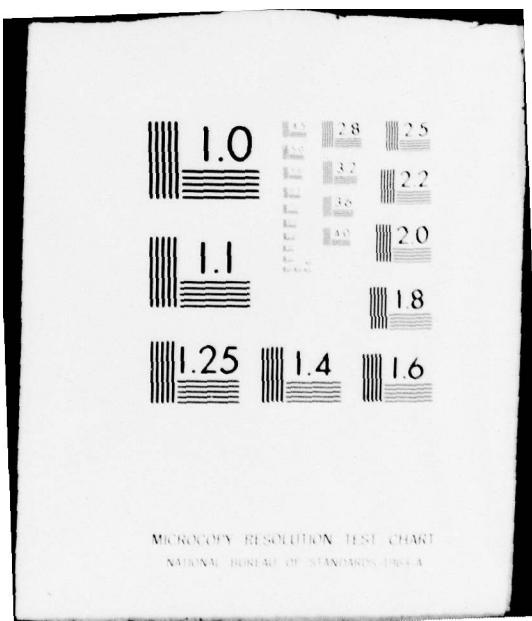
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FINAL REPORT

KA BAND MICROWAVE INTEGRATED CIRCUIT  
SPDT SWITCH DEVELOPMENT

Prepared by

Dr. Charles Buntschuh

June 1979

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Microwave Associates, Inc.  
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K<sub>A</sub>-BAND MICROWAVE INTEGRATED CIRCUIT  
SPDT SWITCH DEVELOPMENT

1.0 INTRODUCTION

1.1 Program Objectives

The objective of this program was to develop a practical broad band, integrated circuit K<sub>a</sub>-band single-pole-double-throw switch with driver with the following performance requirements:

	<u>Design Requirements</u>	<u>Design Goal</u>
Frequency:	26.5 - 40 GHz	
Power Handling Capability:	2 watts CW	
Insertion Loss:	2.5 dB max.	2.0 dB
VSWR:	1.7 max.	
Isolation:	30 dB min.	40 dB
Amplitude Tracking:	± 0.5 dB	± 0.2 dB
RF Transition Speed:	10 ns	5 ns
Total Switching Speed: (including driver delay)	20 ns	15 ns
Switching Repetition Rate:	Variable to 2 MHz	
Driver Control:	T <sup>2</sup> L, 1 or 2 bits	
Input/Output:	WR-28 Waveguide	

Also, the switch must survive looking into a 2:1 VSWR, and it must be capable of "hot switching".

To meet these objectives, Microwave Associates proposed to build two switches using different microwave integrated circuit (MIC) formats. One switch would be in microstrip, using a Duroid teflon-fiberglass substrate, and the other would be in fin-line, also using Duroid as the integrated circuit material. Both switches are to use a high-Q, plated heat sink diode developed by Microwave Associates Ltd, M/A's English subsidiary.

This report covers the design and performance results on both switches.

### 1.2 Background

There are currently no SPDT K<sub>a</sub>-band diode switches on the market and no SPST switches which cover the full waveguide band. Thus, there has been a great need for the development of a broad band switch suitable for use in new systems which will be operating up to 40 GHz.

For the past several years there has been growing activity in extending MIC techniques into the mm-wave spectrum. Much of this activity has been devoted to exploring the suitability of various MIC transmission line media--including some quite novel forms--for mm-wave applications, and their potentials for low-cost reliable microwave components. Also, improvements in semiconductor device technology are yielding diodes of exceptionally high cutoff frequencies, such that MIC circuits using unencapsulated chips will be capable of low-loss broad-band operation well into the mm-wave region.

Figure 1.2.1 shows the cross-sections and configurations of most types of transmission lines, either in wide use or under active investigation for use in the mm-wave region. Figure 1.2.2 compares several of these lines with respect to a number of properties pertinent to various applications. They are listed in order of decreasing Q. These Q's are representative values to be expected in  $K_A$ -band; actual values could vary considerably, depending on size, materials, surface finish, etc.

The most important transmission medium properties for the switch application are its suitability for mounting chip diodes, intercircuit isolation, and the potential for low production cost. Low line loss and ease of transitioning to waveguide are also quite desirable. Microstrip and fin-line were selected for the switch development because they possess favorable combinations of the desired properties. Suspended substrate stripline was also a strong contender, except that it is not as convenient for shunt-mounted diodes, which are preferred over series diodes for switches.

Conventional microstrip, that is alumina substrate microstrip, loses its appeal above  $K_u$ -band because, as the substrate thickness is reduced with increasing frequency to control its tendency to radiate, the line widths become very narrow and the line losses become unacceptably large. This problem is alleviated using low dielectric constant substrates such as teflon fiberglass or quartz. The applicability of Duroid material through  $K_a$ -band and beyond has been amply demonstrated by Rubin and Saul<sup>(1)</sup> of the Naval Ocean Systems Center, and it is gradually coming into

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(1) David Rubin and David Saul, "mm-wave MICs Use Low Value Dielectric Substrates", Microwave Jnl. Vol 19, No. 11, Nov 76, P35.

NON-TEM LINES



WAVEGUIDE



DIELECTRIC WAVEGUIDE



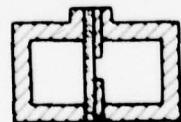
IMAGE LINE



MICROGUIDE



SLOT LINE

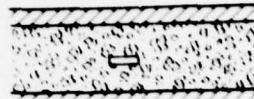


FIN LINE

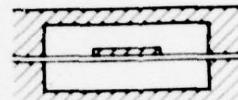
TEM & QUASI-TEM LINES



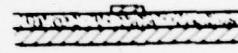
COAXIAL LINE



DIELECTRIC-LOADED STRIPLINE



SUSPENDED SUBSTRATE



MICROSTRIP



TRAPPED INVERTED MICROSTRIP



COPLANAR WAVEGUIDE

FIGURE 1.2.1 MICROWAVE TRANSMISSION LINE CROSS-SECTIONS

	Q	TRANSITION TO WG	ISOLATION PKGD	CHIF	SEMI-COND DEVICE MOUNTING	BEAM LEAD FILTER	3 dB HYBRID	20 dB CPLR.	GUNN RES.	RADIATION FROM DISCONTINUITIES
METAL WAVEGUIDE	3000	-	4	4	1	1	4	3	3	4
IMAGE LINE	2500	3	1	2	1	1	1	1	2	1
SUSPENDED STRIPLINE	600	3	3	2	2	1	3	3	4	1
FIN LINE (DUREON)	500	4	4	1	2	3	4	1	3	2
MICROSTRIP (DUREON)	300	3	2	2	3	4	2	3	4	2
TIM LINE (ALUMINA)	300	1	2	2	3	4	2	3	4	2
CO PLANAR LINE	150	1	2	1	3	4	1	1	2	2
SLOT LINE	100	3	1	1	3	4	1	3	3	2

4 = EXCELLENT

3 = GOOD

2 = FAIR

1 = POOR

(ADAPTED FROM PRESENTATION BY U. GYSEL, FORMERLY OF STANFORD RESEARCH INSTITUTE, AT THE SOLID STATE MM-WAVE TECHNOLOGY WORKSHOP, SAN DIEGO, CA, JUNE 21, 1977.)

FIGURE 1.2.2 COMPARISON OF MM-WAVE MIC TRANSMISSION LINE MEDIA

widespread use in the mm-wave bands. Also Duroid microstrip is being used routinely in broadband switches up through 18 GHz. Thus, it is a logical choice for a circuit medium to extend MIC switch technology up to 40 GHz.

Fin-line has recently received much attention for mm-wave MIC applications including attenuators,<sup>(2),(3),(6)</sup> mixers<sup>(4)</sup> oscillators<sup>(3),(5)</sup> and switches,<sup>(3),(6)</sup> Duroid, clad either on one side (unilateral fin line) or on both sides (bilateral) is normally used as the fin-line material.

The switch development reported on in Refs (3) and (6), has been essentially concurrent with that reported here. The two approaches are different, in that the former used unilateral fin-line with beam lead PIN diodes, whereas the present work uses bilateral fin-line with plated-heat-sink diodes applied with chip-and-wire-bond techniques. The different results obtained from these two approaches will be contrasted in Section 5.3.

---

(2) P. Meier, "Planar Multiport Millimeter-Integrated Circuits", MTT Symposium Digest, p385, June 1977.

(3) H. Hofmann, H. Meinel, B. Addseck, "New Integrated mm-Wave Components Using Fin Lines", MTT Symposium Digest, p21, June 1978.

(4) G. Begemann, "An X-Band Balanced Fin-Line Mixer", MTT Symposium Digest, p24, June 1978.

(5)

L. Cohen, P. Meier, "Advances in E-Plane Printed Millimeter-Wave Circuits", MTT Sympsoium Digest, p27, June 1978.

(6) H. Meinel, B. Rembold, "New Millimeter-Wave Fin Line Attenuators and Switches", MTT Symposium Digest, p249, April 1979.

## 2.0 MICROSTRIP SWITCH DESIGN

### 2.1 Design Considerations

In developing a broadband K<sub>a</sub>-band microstrip switch, the following important design considerations must be taken into account:

- a. The design of a broadband waveguide-to-microstrip transition.
- b. The choice of series or shunt diodes, or a series-shunt combination.
- c. The number of diodes to be used in each arm.
- d. Diode selection, with respect to junction capacitance, series resistance, I-layer thickness, and thermal resistance.
- e. Construction techniques suitable for low production costs.

For the transitions, we chose to use a cosine taper to a ridge guide microstrip launcher similar to the design reported by Saul.<sup>(1), (7)</sup> The transition is discussed in detail in Section 2.2

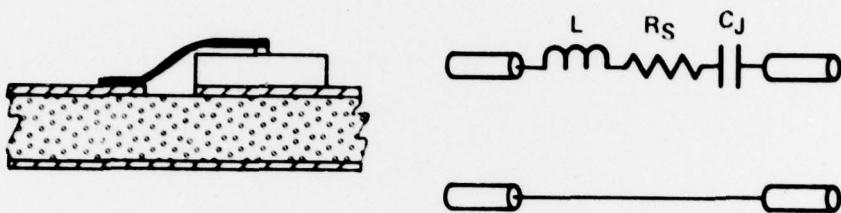
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<sup>(7)</sup> D. Saul, "Wideband Microstrip Components and the IFM Discriminator", Proc 1974 Millimeter Wave Techniques Cont., Vol 2, p D4-1, 12.

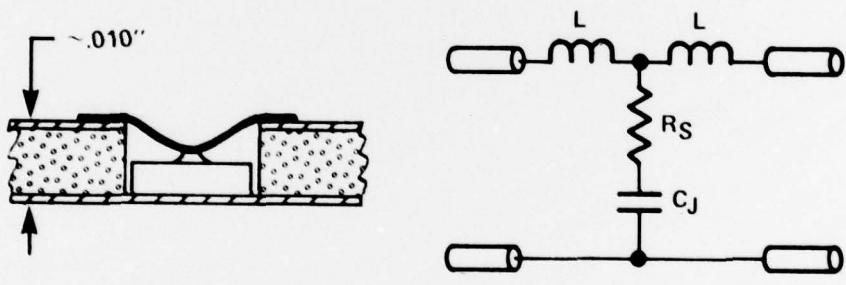
The mounting configurations for series and shunt chip diodes in microstrip with a nominal .008" dielectric thickness are shown, roughly to scale, in Figure 2.1.1. The equivalent circuits for the zero or reversed biased state are also shown; the circuits for the forward biased state are the same, but with the junction capacitance shorted out.

Series diodes are much easier to mount since holes through the circuit board are not required. Also the series inductance can be much less than for shunt diodes since only one strap is needed. A series-diode SPDT switch has much broader bandwidth capability than a shunt diode switch, since the first diode is located right at the junction. The disadvantage of the series diode is that switch isolation depends upon the diodes' capacitance, and it is essentially impossible to obtain a useful amount of isolation at  $K_a$ -band from diodes with the lowest practicable capacitance.

Figure 2.1.2 illustrates this point. It compares the calculated insertion loss and return loss in the pass state, and isolation of single series and shunt diodes from 20 to 40 GHz in a 50 ohm system for  $C_j = .03 \text{ pF}$ ,  $R = 1 \text{ ohm}$ , and  $L = .12 \text{ nH}$ . (At 33 GHz, mid  $K_a$ -band, .03 pF is 160 ohms and .12 nH is 25 ohms of reactance.) The insertion losses of both are about the same, limited essentially by the mismatch caused by the series inductance; the series diode is slightly better because of the lower inductance. Increasing the series resistance to 3 ohms increases the insertion loss of the shunt diode by less than .02 dB whereas that of the series diode increases by about 0.2 dB. The isolation, on the other hand is approximately 30 dB for the shunt diode, limited primarily by the diode series resistance, and as low as 3.5 dB for the series diode. Even reducing  $C_j$  to .01 pF, which is probably not practical, at least for high-speed switch, would only increase the isolation to 11.5 dB at 40 GHz.



(a) SERIES



(b) SHUNT

**FIGURE 2.1.1 CONFIGURATIONS AND EQUIVALENT CIRCUITS FOR  
SERIES & SHUNT MOUNTED CHIP DIODES IN MICROSTRIP.**

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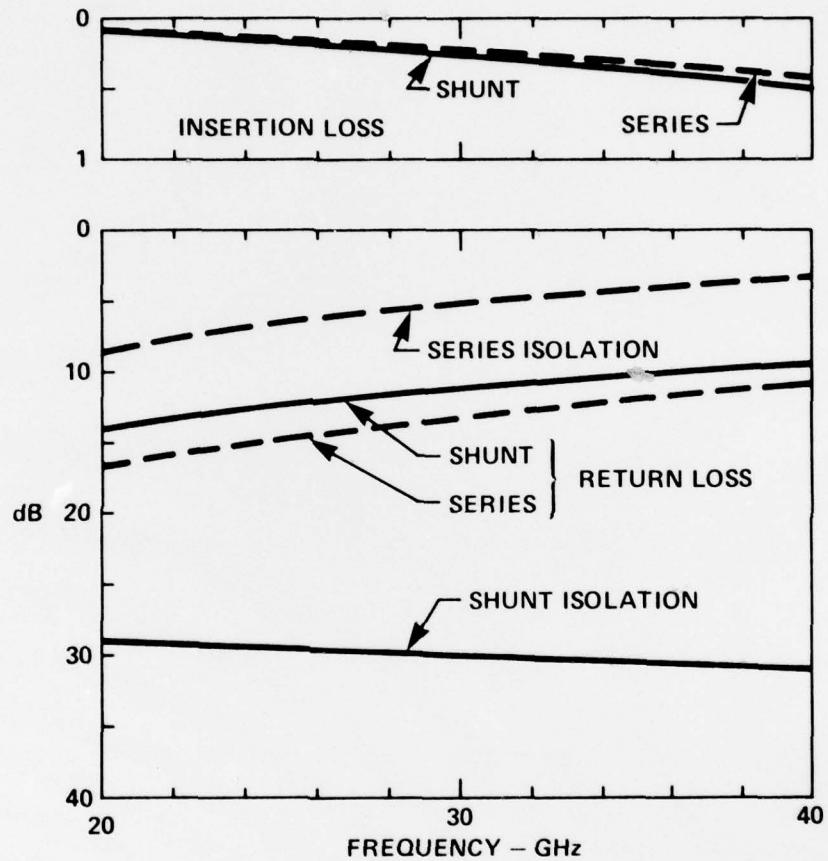


FIGURE 2.1.2 CHARACTERISTICS OF .03 pF, 1Ω DIODE IN SERIES AND SHUNT MOUNTING

D-17030

Figure 2.1.3 compares the characteristics of series and shunt diodes in 2-diode SPST switches. The parameters are the same as in Figure 2.1.2, and the spacing was chosen to match the pairs near 33 GHz. The isolation of the shunt diode switch is about 65 dB; even with  $R_s = 3$  ohms, it will still be about 45 dB. The series diode isolation runs from 22 down to 7 dB; its insertion loss is also .1 - .2 dB higher than that of the shunt switch. Clearly, it is essential that shunt diodes be used for a K<sub>a</sub>-band switch. Also, these results indicate that two diodes in each arm of a SPDT switch should be adequate from the standpoints of insertion loss, isolation and bandwidth.

The return loss at the band edges, calculated for a SPST with 0.12 nH series inductance is only about 1 dB higher than desired for a complete SPDT switch. The effect of the wire bond inductance on the insertion loss and match of a shunt diode SPST switch is shown in Figure 2.1.4. Here again the spacings were chosen to match the pair near 30 - 33 GHz. For .04 nH, the match would be better than 40 dB and the insertion loss would be negligible. Such a low inductance is, however, beyond a practical limit. Small capacitance diodes have very small top contacts--typically under .001" in diameter--so that the bonding must be done with fine, high inductance wire. Consequently, using .0007" diameter bonding wire, we expect the minimum inductance to be in the .10 - .15 mH range. Also, in fabricating the switch it is important to keep the leads as short as possible.

For any shunt diode switch, low series resistance is desired for high isolation, and low capacitance for broadband, high frequency insertion loss performance. The preceding calculated results indicate that excellent performance can be obtained with  $C_j \leq .03$  pF and  $R_s$  in the 1-3 ohm range.

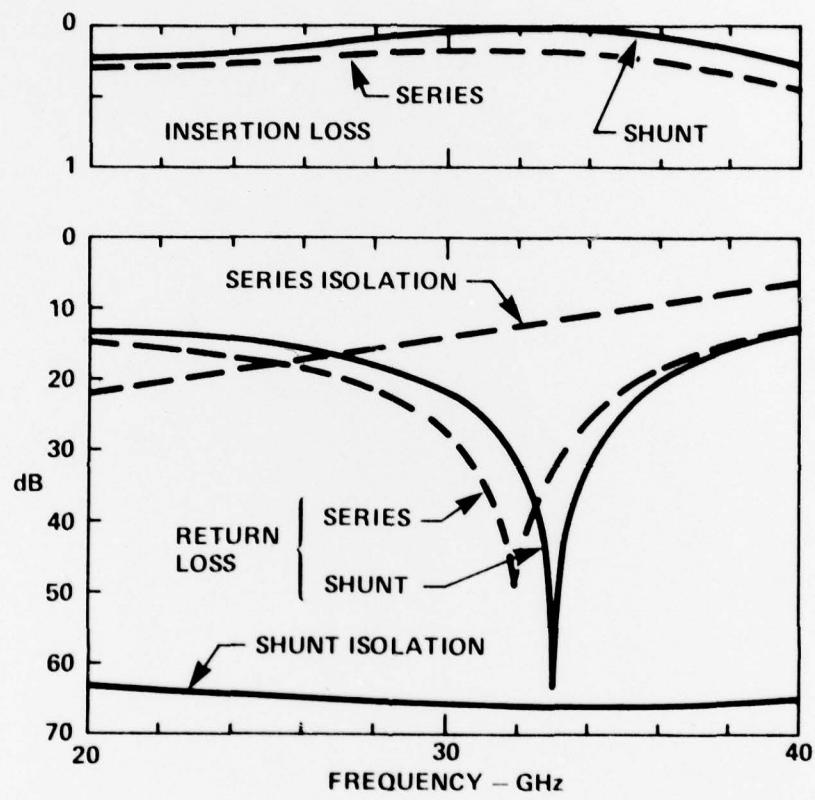
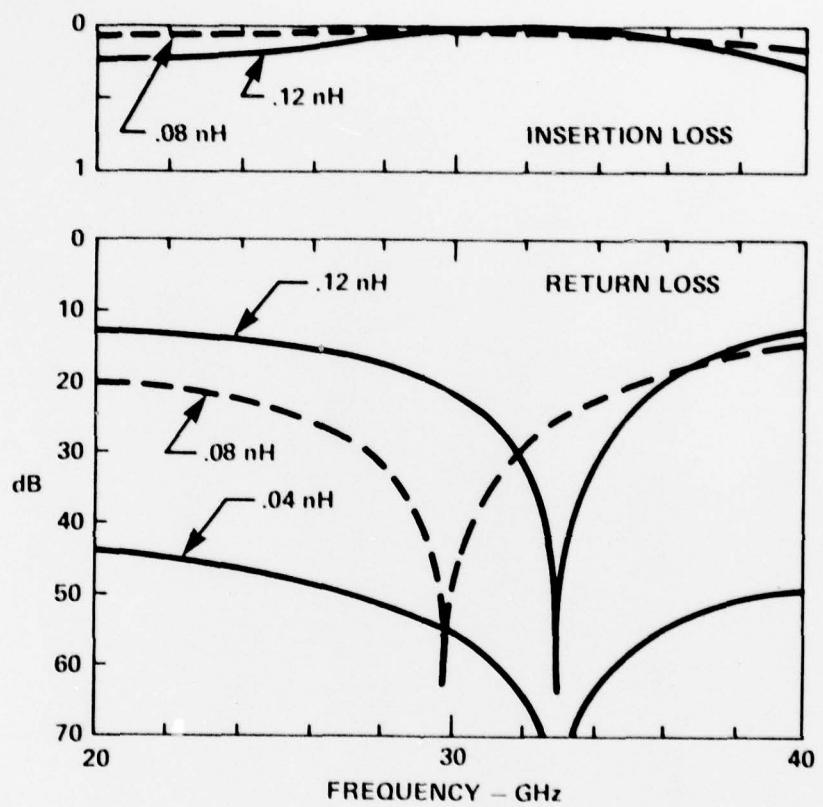


FIGURE 2.1.3 CHARACTERISTICS OF 2-DIODE SPST SWITCHES WITH  
.03 pF, 1 $\Omega$  DIODES IN SERIES AND SHUNT CONFIGURATIONS

D 17022



**FIGURE 2.1.4 INSERTION LOSS & RETURN LOSS FOR TWO SHUNT  
.03 pF, 1Ω DIODES FOR SEVERAL VALUES OF  
SERIES INDUCTANCE**

D 17023

Fast switching speed demands a thin I-layer diode, while high power handling ability requires thick I-layers and low thermal resistance. At the specified 2 watt level, diode burnout is not the power-limiting effect. Rather it is the change in isolation and insertion loss due to non-linear resistance and heating of the diodes. We estimated that a 5  $\mu$ m I-layer diode would represent a reasonable compromise in the switching speed--power handling trade off. Thus, for the switch development, we used an exceptionally high-Q, low capacitance, plated-heat-sink diode developed by Micro-wave Associates Ltd, M/A's English subsidiary. This diode is described in detail in Section 2.3.

The overall switch design is described in Section 2.4. In designing the switch, consideration was given to keeping the ultimate production costs down. In particular, this motivated the choice of plastic substrate, rather than quartz, and it led us to design the waveguide-microstrip transition for low cost production. Also, in Section 6.0 we suggest another transition technique which could further reduce volume production costs substantially.

## 2.2. Waveguide-Microstrip Transition

Single-ridge waveguide forms an excellent, "natural" launcher to microstrip line, since the field and current patterns of the two are quite similar. Rubin and Saul at NOSC<sup>(1)</sup> developed a tapered ridge, transforming from full height WR-28 waveguide to a single ridge gap which mated to a .010" Duroid microstrip board with a 60 ohm microstrip line. We have adapted and modified the NOSC transition design for use in the SPDT switch; Figure 2.2.1 shows a schematic cross-section of the transition as used in the switch.

The shape of the taper is a cosine curve about 1.5" long--about 3 wavelengths at K<sub>a</sub>-band. We increased the amplitude of the cosine to mate with a .008" Duroid board with a 50 ohm line. The ridge is .040" thick. The nose of the launcher is chamfered to approximately the .023" width of the line, to reduce the fringing capacitance of the corner. To match the transition we added a .005" - .010" length of Duroid in the ridge guide gap as shown. In fact, varying this length is the only tuning required to compensate for slight dimensional variations from unit to unit.

In our early experiments we found it necessary to have a narrow channel with a low roof over the microstrip near the launchers to avoid mismatch and radiation effects of higher order modes. Therefore, we have included in the transition unit a short section of reduced height and width guide at the launcher end, forming a small bridge over the microstrip.

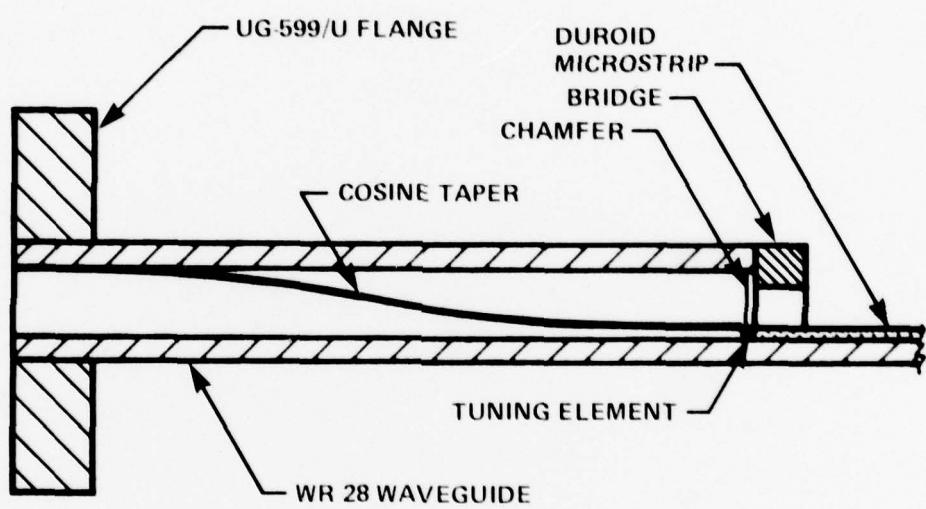
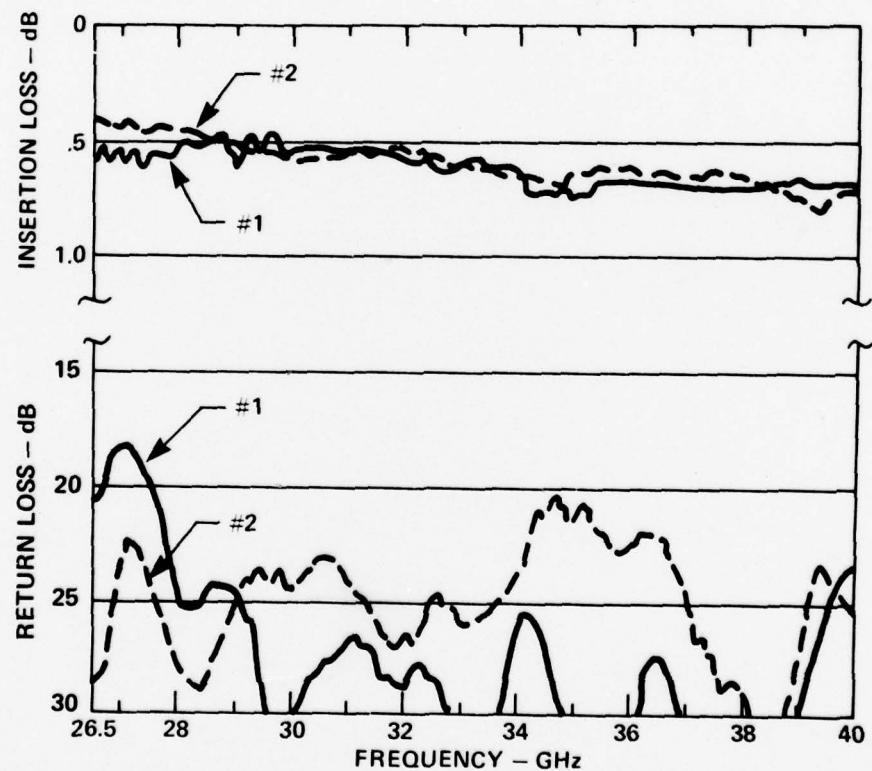


FIGURE 2.2.1 CROSS SECTION OF WAVEGUIDE-MICROSTRIP  
TAPERED TRANSITION

O 17024

We have also redesigned the transition assembly to make it less expensive to manufacture than the NOSC version. The cosine taper, including indexing tabs on each end, is machined out of flat stock on an optical tracing miller, and a standard WR-28 copper guide is slotted in the top wall to take the tapered part. The UG-599/U flange is added and the three pieces are brazed together. The waveguide end is machined off flat, removing one indexing tab. At the launcher end the guide top wall and the indexing tab on the taper are milled off, leaving the side walls and floor as a guide to position the bridge, which is then soldered in place. Finally, the entire assembly is silver plated.

Typical performance of the transition is given in Figure 2.2.2, which shows the loss and match of back-to-back pairs of transitions, separated by 0.5" of 50 ohm microstrip line, for two different assemblies. The return loss of the pair is typically much better than 20 dB over the band. The insertion losses of the circuits ran 0.5 to 0.7 dB from 26.5 to 40 GHz, most of which is due to the microstrip line. We did not attempt to evaluate the individual loss contributions of the line and transitions.



**FIGURE 2.2.2 INSERTION & RETURN LOSS OF TWO MICROSTRIP TEST FIXTURES WITH 0.5" OF DUREON MICROSTRIP LINE**

D-17025A

### 2.3 Plated Heat Sink Diode

The plated heat sink (PHS) diode construction developed at Microwave Associates Ltd. can best be understood by reference to Figures 2.3.1 and 2.3.2 which illustrate and compare the conventional and PHS mesa diode structures. A conventional PIN diode is made by growing the I-layer on an N+ substrate, and diffusing the P+ layer into the surface of the epitaxial layer. The back of the N+ layer is completely metalized and small dots on the P+ side are metalized prior to etching the mesas. In the PHS technique, the P+ side is metalized entirely and then plated up with several mils of copper and then gold plated. Next, the unmetalized N+ layer is thinned to a fraction of a mil by etching, and then the dots are metalized on the remaining N+ material, followed by the etching of the mesas.

The resulting diode has a significantly lower series resistance,  $R_s$ , than the conventional diode by virtue of almost eliminating the contribution of the N+ substrate. Series resistances around 1.5 ohms at 10 mA forward bias for junction capacitances in the .02 - .05 pF range are typical. Thus switching cutoff frequencies of > 2000 GHz are attained at 10 mA whereas cutoff frequencies < 1000 GHz at 10 mA are typical for conventional mesa diodes. Conventional diodes can sometimes be driven into saturation with about 100 mA of bias to bring its resistance down to comparable values, but the switching speed will suffer correspondingly.

The PHS construction also has the obvious advantage of a very low thermal resistance from the junction to the mounting surface in the microwave circuits, since the normal thermal path through silicon is replaced by copper, which has almost

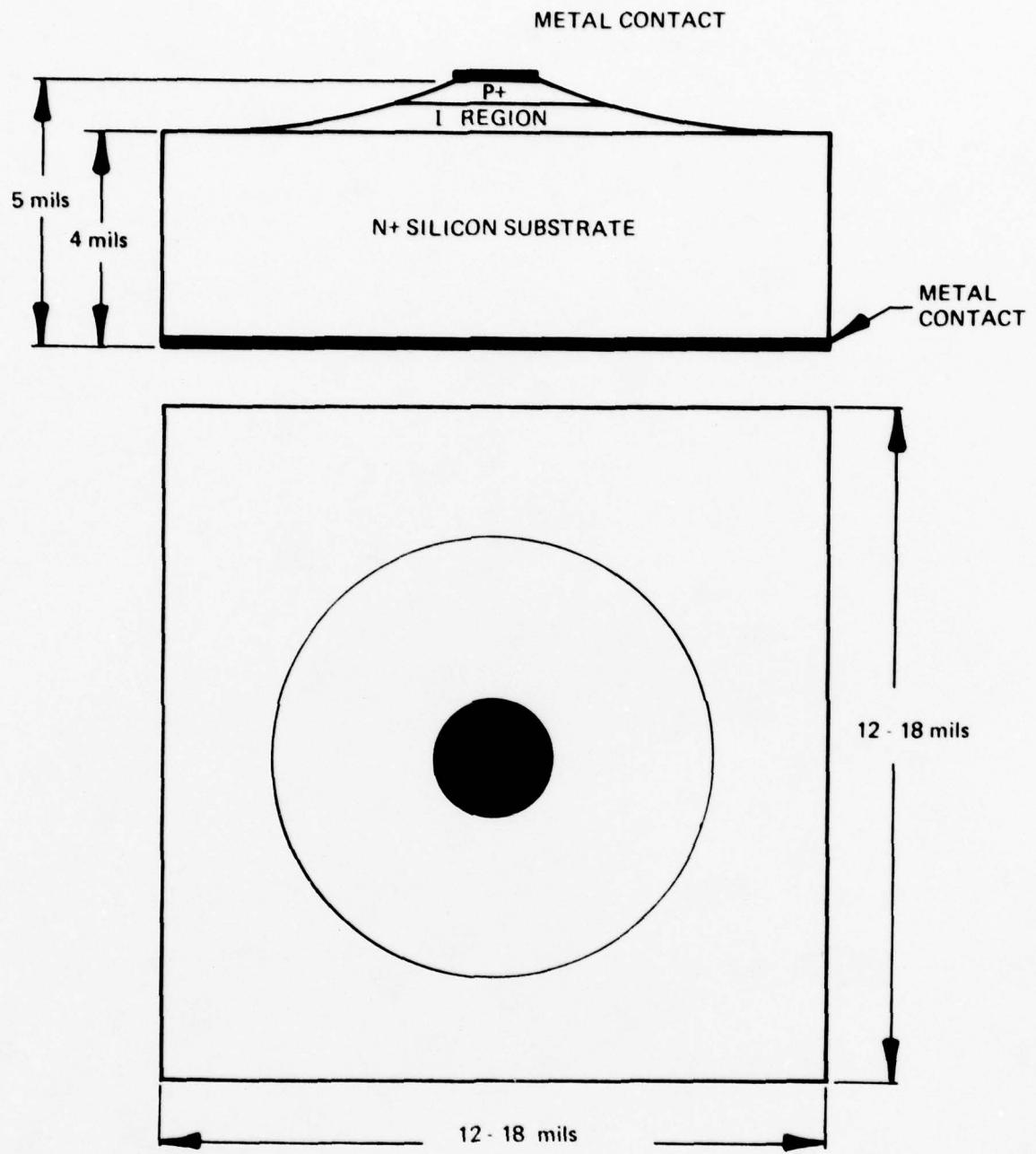


FIGURE 2.3.1 SILICON PIN DIODE CHIP

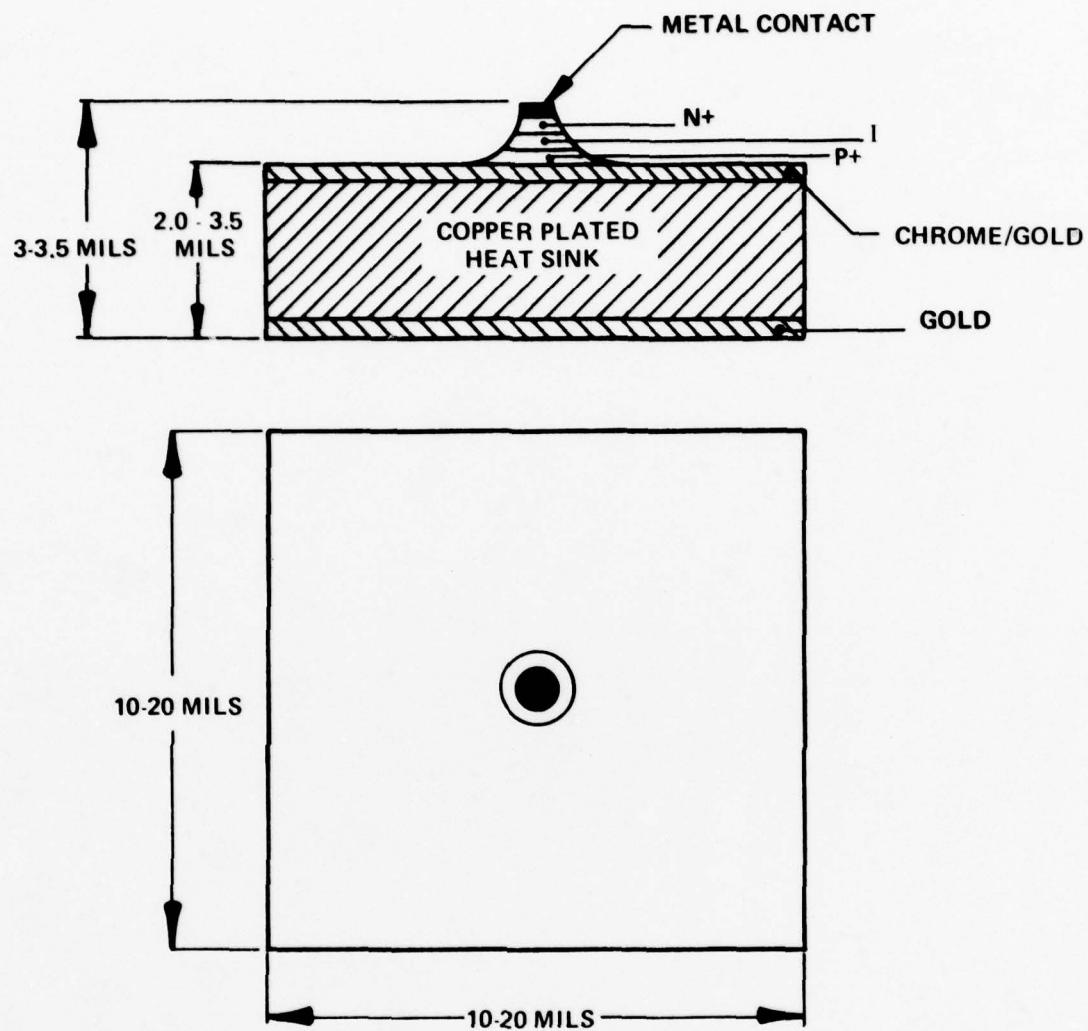


FIGURE 2.3.2 SILICON PLATED HEAT SINK (PHS) NIP DIODE CHIP

5 times higher thermal conductivity. Thus, for circuits in which the diode is mounted on an adequate heat sink, such as shunt mounting in microstrip or stripline, the circuit will handle substantially higher average power than the conventional diode. In a typical installation the thermal resistance is roughly halved and the power handling doubled.

The PHS diode has reversed polarity, that is it is a "NIP" rather than a "PIN" diode. This necessitates using a reversed polarity driver or isolating the diode mount from dc ground. Since the driver we use provides both positive and negative outputs, we have employed the reversed polarity approach.

Pafford of Microwave Associates Ltd. reported on SPST switches in the 55-75 GHz range, using the PHS diode in a ridge-guide circuit.<sup>(8)</sup> He achieved 5 percent bandwidths with 1.0 - 1.2 dB insertion loss and 23-25 dB isolation in a single diode switch. He estimated that the switch, with 3  $\mu$ m I-layer diode, would handle at least 1 watt CW. Also the diodes were gold-doped to reduce the carrier lifetime and enhance the switching speed; RF transition time under 1 ns were achieved.

For the K<sub>a</sub>-band MIC switch, where a 2-watt capability is desired, with a 5 ns switching speed, we chose a slightly thicker diode, and eliminated the gold doping. We estimated that a 4-5  $\mu$ m diode would handle the 2 watts without suffering insertion loss degradation with 5 volts of reverse bias applied in the pass state. Also, since the driver will switch a 8  $\mu$ m non-gold-doped diode in under 5 ns, we could forgo the doping, which improves the diode series resistance at low forward currents.

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<sup>(8)</sup> A. Pafford, "An "O" Band Fast PIN Diode Switch", Proc. 1976 European Microwave Conference, p674.

The PHS diodes delivered for this program were specified by Microwave Associates Ltd to have the following parameters:

Junction Capacitance:	$C_j = .02 - .03 \text{ pF}$
Series Resistance:	$R_s = 1.0 - 1.5 \text{ ohms}$
Breakdown Voltage:	$V_B \geq 90 \text{ V}$
Carrier Lifetime:	$\tau \leq 90 \text{ ns}$
Thermal Resistance:	$\theta \approx 40 \text{ }^{\circ}\text{C/W}$

Furthermore, these diodes were punched-through at zero bias, so that it is not necessary to apply any reverse voltage to minimize insertion loss

## 2.4 Driver

The switch driver is the MA8417-203, a thin film integrated circuit driver developed at Microwave Associates for high speed, high clock rate applications. It is in an hermetically-sealed dual in-line ceramic package and is readily integrable into the microwave package.

Figure 2.4.1 is a circuit schematic of the MA8417. Note that it has complimentary inverting and non-inverting outputs. Thus with the outputs wired to opposite sides of the switch, one side will be reverse biased to 5V, and the other will be forward biased to approximately 30 mA. The forward current can be reduced to any desired value by adding an external current limiting resistor. Each output is divided into a resistive and a capacitive terminal. If the two output terminals are tied together, approximately 150 mA of spiking current is fed through the capacitive lead to obtain fast switching speeds. In our switch, we used the resistive output only, and did not add an external limiting resistor.

This driver may be biased by either  $\pm$  5V or  $\pm$  12V supplies; we provided leads only to the  $\pm$  5 Volt terminals on the final switch. It operates from 2-bit TTL logic. A logic "1" input yields a positive voltage (reverse bias on our PHS NIP diodes) on the non-inverting output. It is also rated to operate over the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range.

The MA8417-203 will switch an 8  $\mu\text{m}$  thick PIN diode from 30 mA to 5V with an RF rise time under 5 ns and a total time, including delay of under 10 ns. The switching rate is conservatively rated at 15 MHz, although it will operate acceptably up to 20 MHz.

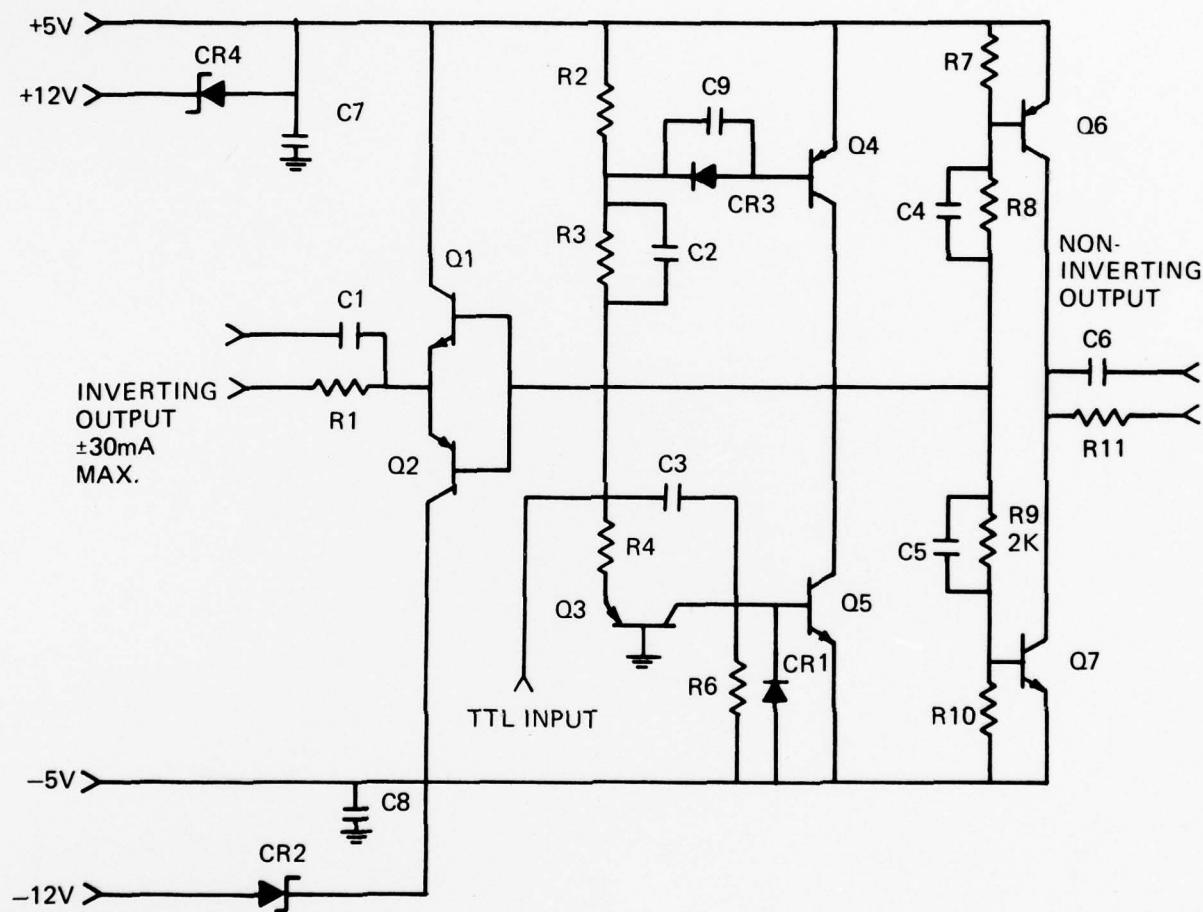


FIGURE 2.4.1 MA8417-203 SPDT COMPLIMENTARY OUTPUT DRIVER SCHEMATIC

## 2.5 Switch Design

The layout of the microstrip portion of the switch is shown in Figure 2.5.1. The circuit fits in a narrow channel in the housing, and each arm mates with a launcher as shown in Figure 2.2.1. As one might expect, the design is very much like a microstrip switch at lower frequencies. The principal differences are the details of the diode mounting, the bias network, and, of course, the launchers.

We experienced some difficulty with the dc block, and we explored numerous possibilities before finding a suitable solution. The design selected consists of a .010" thick metalized titanium oxide ceramic chip, mounted on edge in a .010" gap in the line as shown in the cross-sectional view. These blocks have very low loss and, although they do tend to mismatch the line slightly, they can be readily tuned with short stubs. Figure 2.5.2 shows the response of a 50 ohm line between two transitions with four dc blocks in place (with additional tuning). The loss penalty for the four blocks is roughly 0.1 dB, and the return loss is better than 18 dB across the band.

The diodes in each arm should be electrically spaced  $90^\circ$  apart and the first diode should be  $90^\circ$  from the T-junction, at the center frequency of 33 GHz. The electrical lengths of the microstrip lines, and the physical spacings must be adjusted to compensate for the effective lengths of the diode bond wires and the blocking capacitors adjacent to the tee. We determined the spacing empirically. The final values are consistent with the optimum spacing calculated for a bond wire inductance of 0.12 nH and a negligible line length for the dc block.

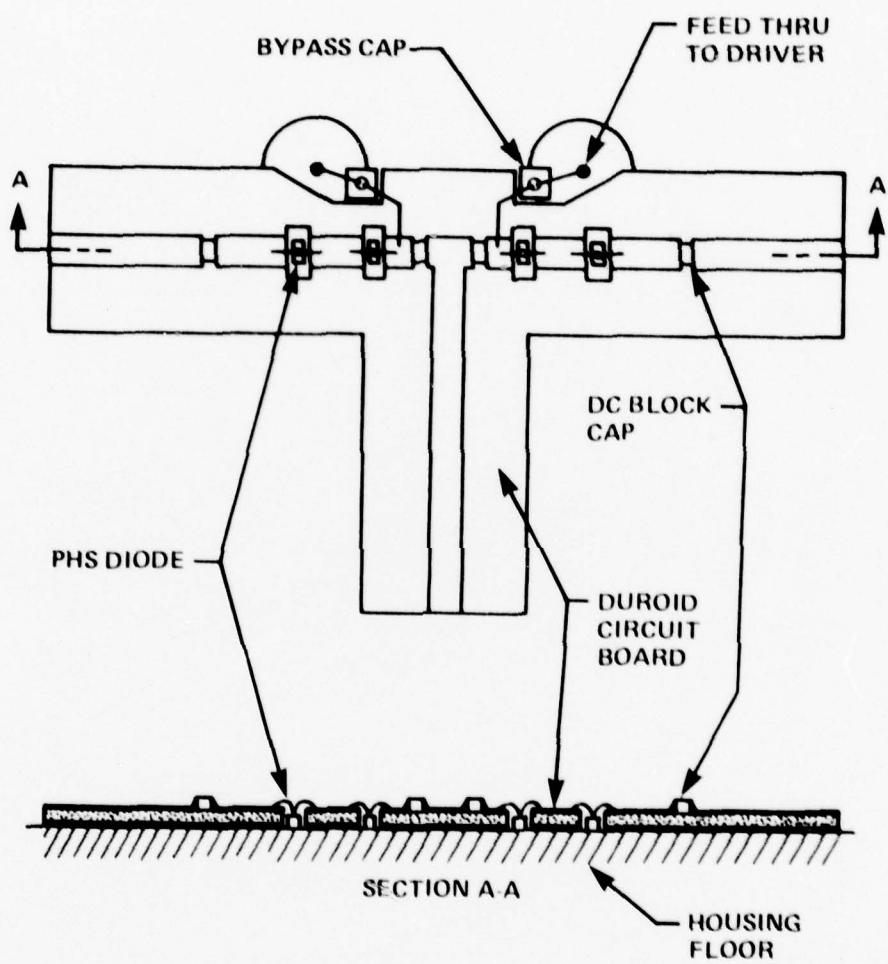


FIGURE 2.5.1 CIRCUIT BOARD LAYOUT OF MICROSTRIP  
SPDT SWITCH

D 17020

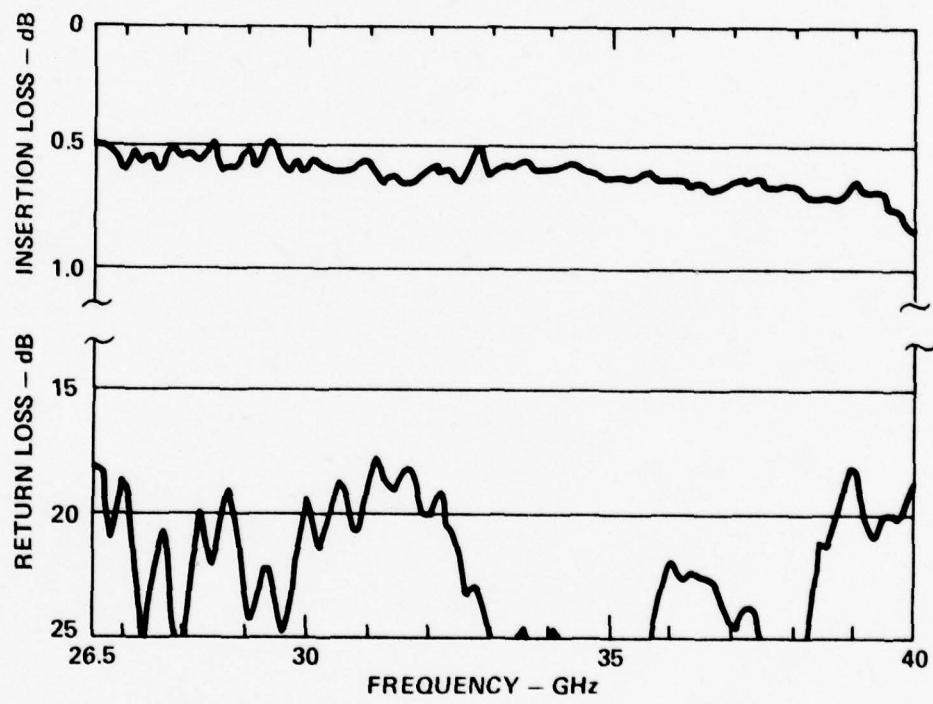


FIGURE 2.5.2 RESPONSE OF  $50\Omega$  LINE WITH DC BLOCKS IN FINAL SWITCH HOUSING

D-17021A

The PHS diodes are about 1/3 the thickness of the circuit board. To help minimize the bond wire length and to make the diodes more assessible for bonding, they are mounted on shims which raise the ground plane in the holes by 3-4 mils. Because the area around the diode mesa is copper and not  $\text{SiO}_2$  as on conventional chips, extra care must be taken to insure that a bond wire does not touch this base and short out. Thus, the diodes are best mounted 3-4 mils below the top of the microstrip line. Contact is made to the diodes and the microstrip line with .0007" gold wire.

The bias networks consist of .0007" gold wires approximately a quarter wavelength long from the microstrip line to 20 pF alumina chip by-pass capacitors and to the feed-thru terminals located at the edge of the board. The feed thrus lead through the housing floor to the driver housing below. Broadband, low frequency switches use miniature multiturn coils for bias chokes, however these cannot be used here since K<sub>a</sub>-band is well above the self-resonant frequency of any such coil.

The complete switch is shown in Figure 2.5.3. The main housing is 1.5 x 1.2 x 0.44". The overall size, including launchers, flanges, and connector is 3.64 x 2.47 x 0.75, and it weighs about 3 ounces. The waveguide inputs are humidity sealed with teflon-fiberglass windows.

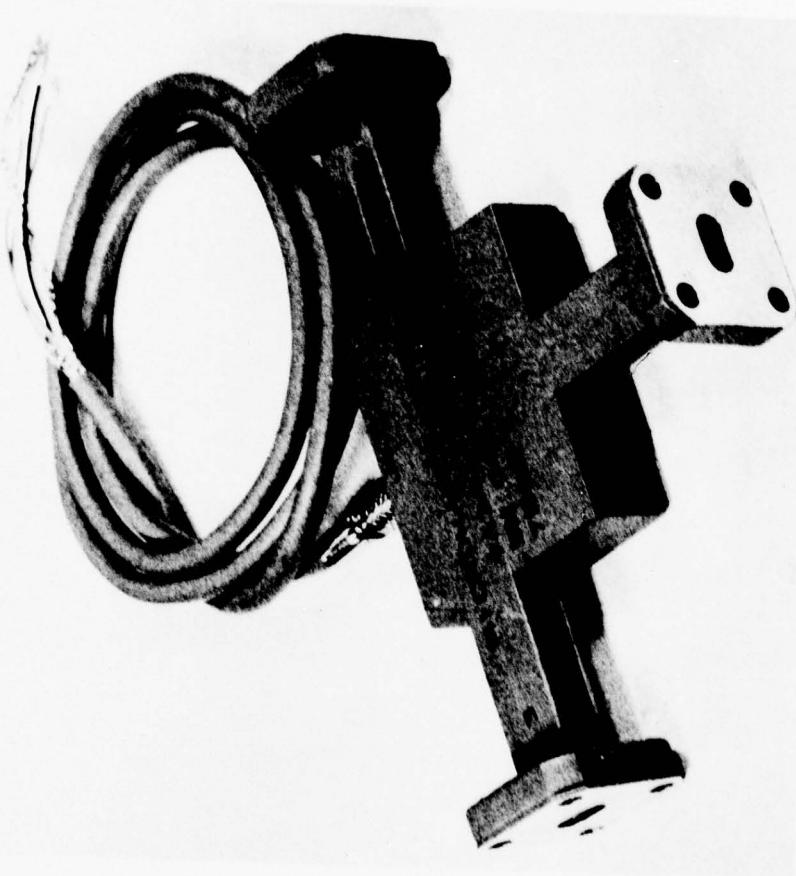


FIGURE 2.5.3 KA-BAND SPDT MICROSTRIP SWITCH

D.17026

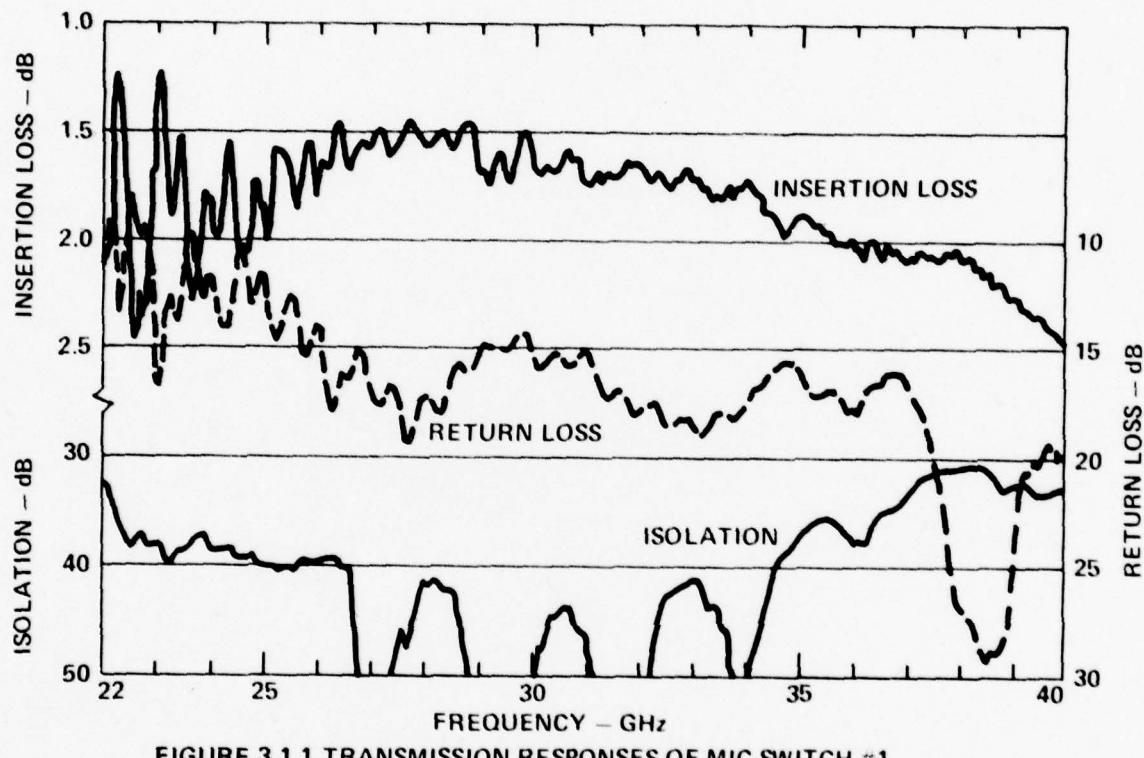
### 3.0 EXPERIMENTAL RESULTS - MICROSTRIP

#### 3.1 Switching Performance

Figures 3.1.1 and 3.1.2 show the insertion loss, return loss, and isolation performance in each state over the 22 to 40 GHz range. The switch was tuned while observing only the 26.5 to 40 GHz responses; we then recorded the responses down close to waveguide cutoff simply to see what the resulting performance was.

Over the 26.5 - 40 GHz design band the insertion loss for both throws is under 2.5 dB, the return loss is better than 14 dB (VSWR < 1.5) and the isolation is greater than 30 dB. The insertion loss tracking of the two arms is within 0.4 dB.

The insertion loss rolls off above 30 GHz from approximately 1.4 to 2.3 dB in one direction and 1.6 to 2.4 dB in the other. This roll off is somewhat greater than should occur due to the normal increase in loss with frequency. We would expect the maximum loss due to this cause to be in the 1.9 - 2.1 dB range. In fact, the J1-J2 arm exhibits such behavior up to 38 GHz, above which the loss rather abruptly increases. The excess loss cannot be attributed to high bond wire inductance or other mismatch, since the match actually improves in this region. It also does not appear to be due to higher order modes or radiation, since the structure should be cutoff to the higher modes and the behavior is the same with and without the cover plate.



**FIGURE 3.1.1 TRANSMISSION RESPONSES OF MIC SWITCH #1,  
J1 TO J2. REFLECTION RESPONSE CORRESPONDING  
TO INSERTION LOSS CASE.**

D 17017

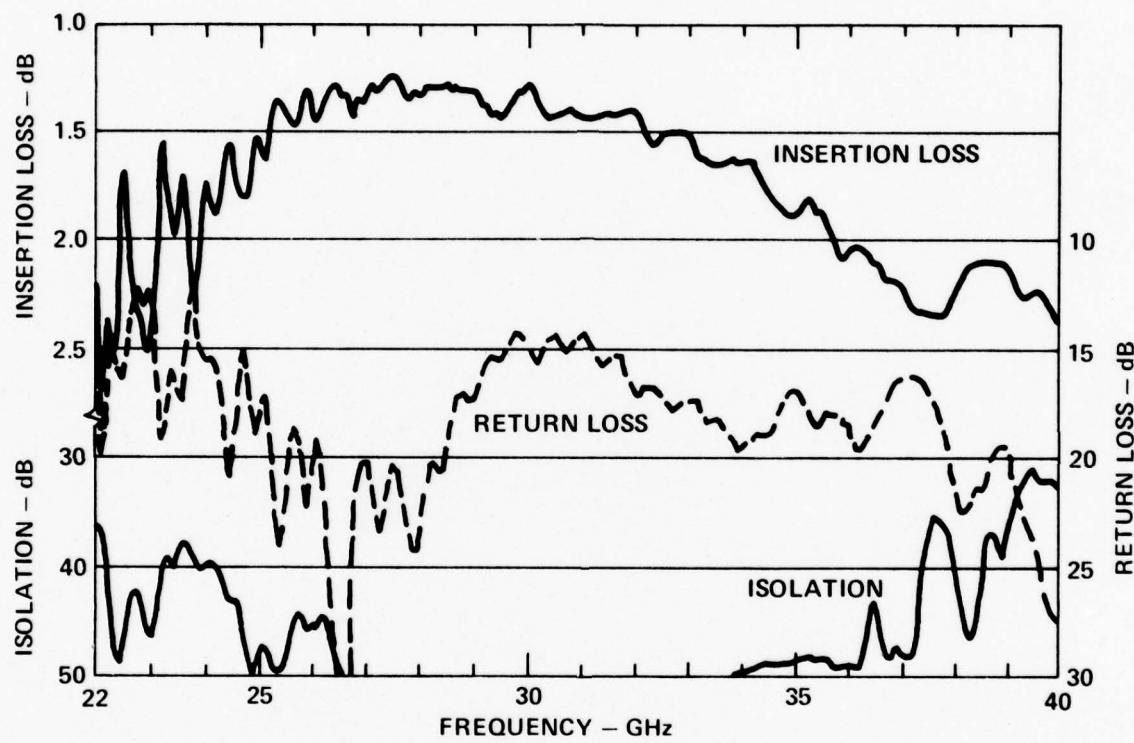


FIGURE 3.1.2 TRANSMISSION RESPONSES OF MIC SWITCH #1,  
J1 TO J3. REFLECTION RESPONSE (CORRESPONDING  
TO INSERTION LOSS CASE.)

D-17016A

We were not successful in determining the cause of this excess loss on this program, but we suspect that there is a low-Q lossy resonance associated with the launcher-bridge area. Clearly, eliminating this loss contribution could improve the insertion loss at the high end by 0.3 to 0.4 dB, bringing it close to, or within, the 2.0 dB design goal.

The maximum isolation was well over 50 dB, (system sensitivity was approximately 55 dB) which implies that the diode series resistance is, in fact, under 2 ohms as expected. There are several spurious responses between 27 and 34 GHz in the J1-J2 arm, but the isolation remains above 41 dB. The isolation of both arms degrade below 50 dB below 26.5 and above 34 GHz, with some spots close to 30 dB. The reason for these spurious responses was not explored. One possibility is that the second harmonic output of the sweeper source is much less attenuated by the switch than the fundamental, due to finite inductance in series with each diode.

Below 26.5 GHz, the performance is somewhat obscured by sharp fluctuations in the return loss due to interference between widely spaced mismatches as the WR-28 waveguide cutoff is approached. There is also a general decrease in the return loss, especially when switched to transmit through the J1-J2 arm. Nevertheless, it appears that the microstrip

switch still performs acceptably down to 22 GHz, and that it would only be necessary to extend the bandwidth of the launcher to extend the bandwidth of the entire switch. To cover the full 18-40 GHz range, however, a transition from ridged waveguide or coaxial line, and a transformer section in the T-junction would be required.

The switching transients are shown in Figure 3.1.3 which is traced from sampling oscilloscope photos. The RF turn-off transient--the diodes going from reverse to forward bias--is 1.6 ns for 10 to 90 percent transmission while the turn-on transient takes 3.4 ns. These are both well under the 5 ns design goal, and do not use the current spiking capability of the driver. The bias current was approximately 20 mA.

The driver delays shown are measured from the driver input pin and do not include the delay through the cable. The input pulse to the driver from the HP 8082A pulse generator had a 5<sup>V</sup> amplitude and less than 1 ns risetime when fed to a 50 ohm matched load. The driver loads the pulser such that the rise and fall times are several nanoseconds long, and on the rise, it levels off at 3 volts for 6-8 ns before continuing up to 5 volts. The total switching times shown of 8.4 ns and 18 ns are measured arbitrarily from the 2.5 volt level, i.e. "50% TTL", which is within the required 20 ns speed. Current spiking would shorten the turn-on delay several nanoseconds.

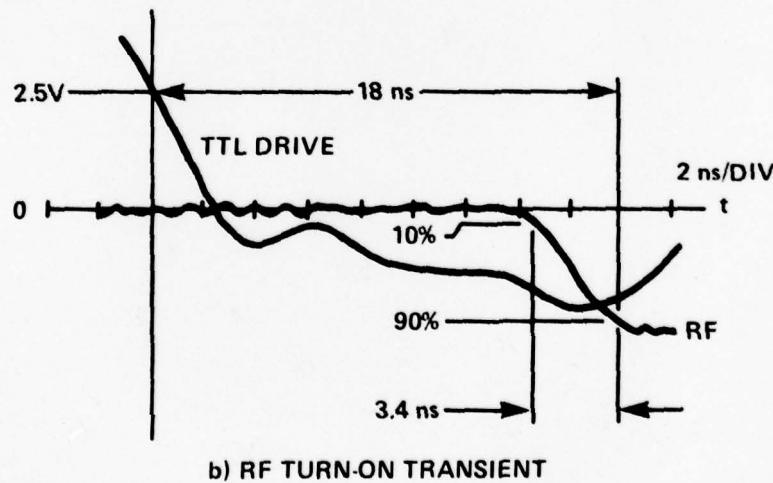
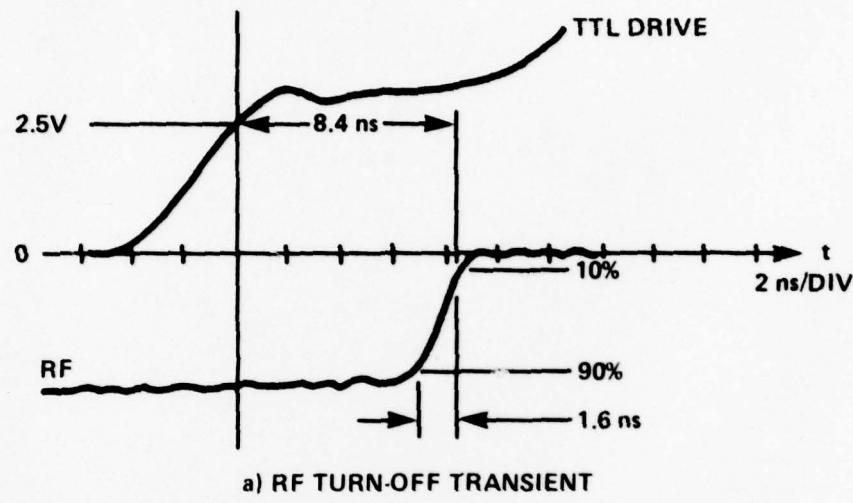


FIGURE 3.1.3 SPDT MIC SWITCH – SWITCHING TRANSIENT

D-17019

### 3.2 Power Handling

Two watts CW at K<sub>a</sub>-band is not generally available. Therefore, in lieu of high power testing the K<sub>a</sub>-band switch directly, we evaluated its performance indirectly at 17.5 GHz. We assembled a 2-diode SPST switch with coaxial input and output, using the PHS diodes mounted as in the K<sub>a</sub>-band switch, but with the diode spacing appropriate to K<sub>u</sub>-band.

Burnout of the PIN diode is not a problem at 2 watts CW, even if the switch were terminated in a short circuit. PIN diodes are safe from burnout in the reverse biased state if the junction temperature remains below 125-150°C and the RF voltage remains below the breakdown voltage. Forward biased diode are safe up to more than 200°C and are relatively immune to burnout. For 2 watts into a switch with 2.5 dB of insertion loss, only 0.9 watts will be dissipated when the output is matched. Roughly one third of this is dissipated in the circuit. The other two thirds is fairly evenly divided among the two reverse biased diodes and the forward biased diode nearest the T-junctions, i.e. about 0.2 watts per diode. Thus, with a thermal resistance as high as 80°C/watt--twice the rated value for the diode--the temperature rise will be only 16°C, well within the safe region even for case temperatures of 70-80°C in a typical military environment.

At 2 watts, the diode RF voltage will be about 15 volts in a matched line and it could be about 30 volts in a shorted line. This is well below the breakdown voltage of 90 volts and is therefore also in the safe region.

At the 2 watt level, the potential high power problem is possible degradation of insertion loss or isolation due to nonlinear effects in the diodes. In the reverse biased

state, carriers are injected into the I-layer during the forward bias half of the RF cycle. At high RF voltages this carrier injection makes the I-region lossy, increasing the effective series resistance of the diode as the RF voltage increases. In the forward bias case, when the RF current approaches the magnitude of the dc bias current, partial carrier sweep out can occur, increasing the series resistance and reducing the isolation. These nonlinear effects become less efficient as the RF frequency increases since the RF period become steadily shorter relative to the carrier relaxation or response times and the carriers become less able to follow the RF voltage. Consequently, we expect high power degradation at  $K_a$ -band to be less than any observed at  $K_u$ -band.

In the SPST test switch, at 17.5 GHz, we measured the variation in insertion loss and isolation with input power up to 2.5 watts input for bias levels of 10V, 0V, 10 mA, and 40 mA. There was no change in insertion loss (i.e. less than 0.1 dB) at 10V and 0V. At 2 watts the isolation decreased by 0.9 dB at 10 mA and 0.5 dB at 40 mA; at 2.5 watts it decreased by 1.9 dB and 0.7 dB at 10 and 40 mA. Thus we expect that the  $K_a$ -band switch will suffer a negligible decrease in isolation at least to the 2 watt level with 10 mA or more bias.

The diodes also survived hot switching up to 2.5 watts. Hot switching was done simply by making and breaking contact with the bias lead, so that the switching speed was governed by the carrier lifetime, about 40 ns in this case, and was therefore much slower than it would be with a fast driver.

Note that the diode voltage at 2.5 watts input is equivalent to the maximum voltage that could occur at 2 watts with a 2:1 output VSWR, in the absence of losses. A similar statement holds for the diode current. Thus, the experiment at 2.5 watts with a matched load represents

a slightly more severe test than 2 watts with a 2:1 output mismatch in terms of the electrical stresses on the diodes.

## 4.0 FIN LINE SWITCH DESIGN

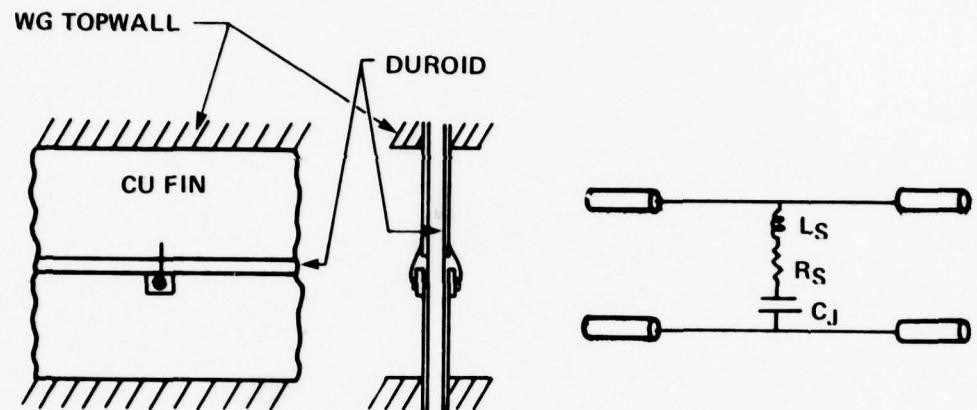
### 4.1 Design Considerations

The same basic design considerations cited for the microstrip switch on p7 regarding transitions, diodes, and construction techniques also apply to the fin line approach. Additionally we must consider the practical range of fin line line impedances, since fin line is intrinsically a higher impedance medium than microstrip.

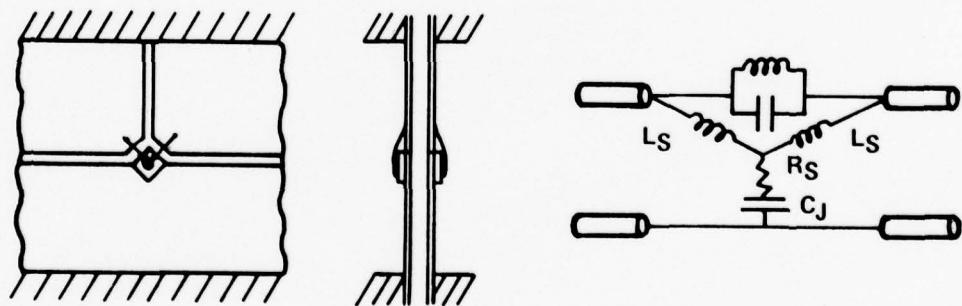
For the waveguide to fin line transition we again chose to use a cosine taper. Its design and performance are described in Section 4.2.

We noted in the microstrip case that a series diode would be preferred were it not for the low isolation, because of the ease of mounting and inherently broader bandwidth. Fortunately, in fin line the shunt-mounting is the easier, and because the fin line T is a series junction, the first shunt diode can be located at the junction, which potentially provides the extra bandwidth capability.

Two methods for shunt-mounting chip diodes in fin line are shown in Figure 4.1.1. In the simple shunt mounting the chips are soldered to one fin next to the gap and a bond wire jumps the gap and makes contact to the other fin. The wire inductance in this case appears in series with the diode, in shunt with the line, which tends to limit the isolation. By cutting a narrow slot in one fin perpendicular to the gap and running a bond wire from each side to the diode, as shown, puts the inductance in series with the transmission line, reducing or eliminating the inductance in the shunt circuit, thereby improving the isolation. The experimentally observed effect of the slots is discussed in detail in Section 5.1.



(a) SIMPLE SHUNT-MOUNTED CHIPS



(b) MOUNT WITH SERIES OPEN CIRCUIT SLOTS

FIGURE 4.1.1. CONFIGURATIONS & EQUIVALENT CIRCUITS FOR SHUNT-MOUNTED DIODES IN FINLINE

D-19033

To maintain symmetry in the bilateral fin line, we mounted diodes on both sides of the circuit board.

Since we wished to obtain a direct comparison of the performance of the microstrip and fin line switches, we chose to use two pairs of diodes in each arm of the fin line switch. The two diodes in each pair are located on opposite sides of the fin line board for symmetry and are thus equivalent to a single shunt diode in microstrip.

#### 4.2 Waveguide-Finline Transition

For the purpose of developing the transitions and for examining the properties of fin line, we built a straight-through, two-port test fixture. Figure 4.2.1 illustrates a typical etched circuit pattern, with a pair of back-to-back cosine tapers to a fin line gap nominally .006" wide at the center. It is printed on both sides of .010" thick Duroid, clad with 1 ounce copper. The total thickness is about .012". Each cosine taper is 1" long; the gap is under .008" for about .300" along the center. The circuit board is clamped between two silver-plated blocks, milled with the waveguide and choke channels, as shown in Figure 4.2.2. Early in the program we had made several circuit boards with a line of plated through holes along the edges of the gap to maintain both sides of the same potential. However, we found no difference in performance without the holes as long as symmetry was maintained by making both side of the board the same. Thus in most experiments and in the switches such symmetry was maintained, and generally plated-through holes were not used.

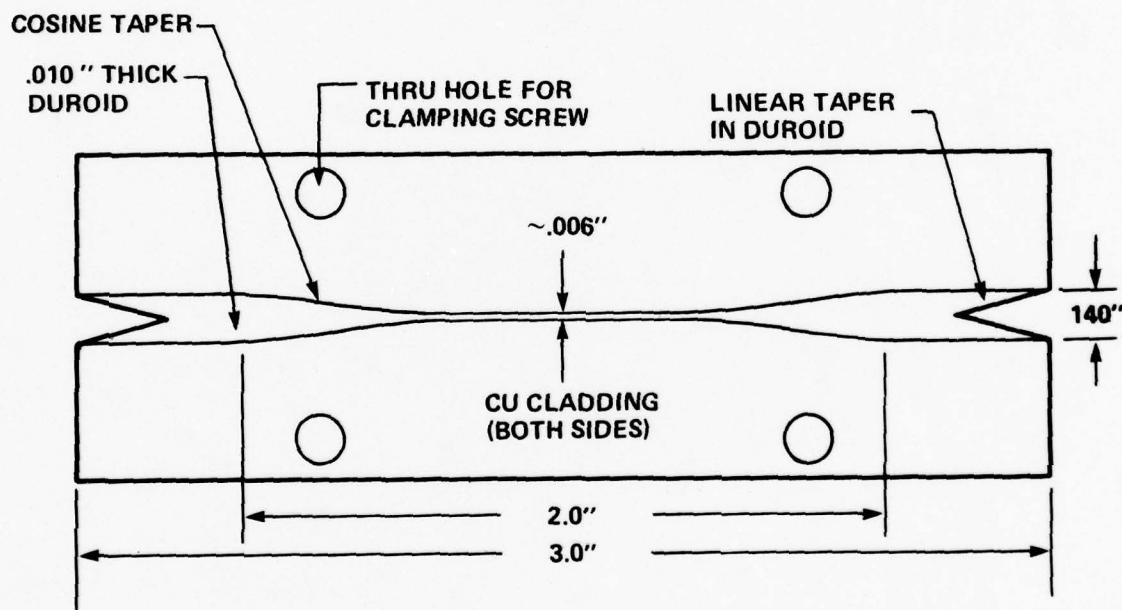


FIGURE 4.2.1. BACK-TO-BACK COSINE TAPERS TO  $60\Omega$  FINLINE  
FROM WR-20 WAVEGUIDE

D-18941

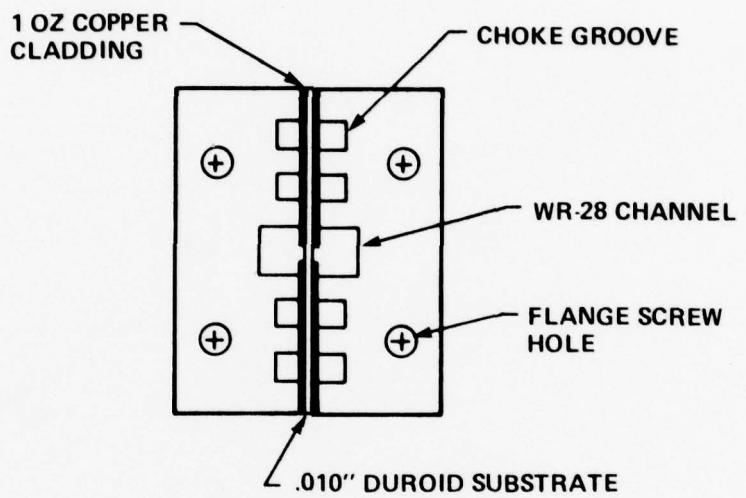


FIGURE 4.2.2. FINLINE SPST SWITCH TEST HOUSING – END VIEW

D-18927

Figure 4.2.3 shows the insertion loss and return loss of the test housing without any fin line substrate, with a dielectric-only fin, and two different tapers. The loss of the empty housing is about 0.1 dB, and the match, which is better than 25 dB over most of the band is essentially that of the detector. Adding a Duroid substrate without any copper in the waveguide adds another 0.1 dB to the loss and does not materially affect the match.

The loss with the 1-inch cosine tapers, with a .007" gap, as in Figure 4.2.1 ran from 0.4 to 0.5 dB, and its match is excellent. Encouraged by this performance, we later made a new circuit with back to back 1/2-inch long tapers. The short-taper circuit had about 0.1 dB less loss than the long taper circuit, and its match was still acceptable.

From these loss measurements, we have estimated the loss of a low impedance gap, .005 - .007", to be about 0.3 dB/in, and a full height gap (Duroid only fin) to be about 0.07 dB/in.

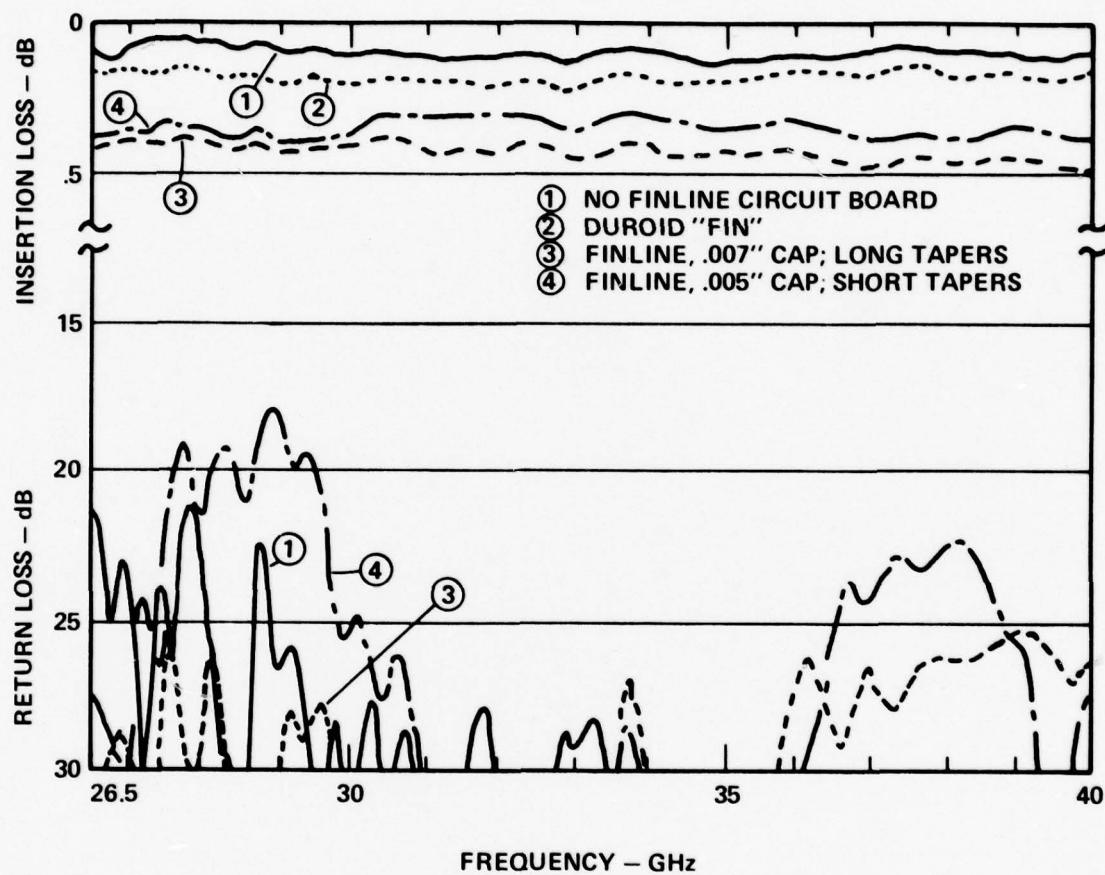


FIGURE 4.2.3. CHARACTERISTICS OF FINLINE TEST CIRCUITS

D-18929

#### 4.3 Finline Impedance

To estimate the characteristic impedance of the fin line circuits we modified a program to compute ridge waveguide impedances to include the effect of the dielectric loading in the gap. The ridge-guide program is based on Hopfer's<sup>(9)</sup> formulation for line impedance (power-voltage definition), utilizing Chen's<sup>(10)</sup> capacitance formula, and Pyle's<sup>(11)</sup> proximity correction. The calculations for the dielectrically-loaded finline follow the formulation of Saad and Begemann<sup>(12)</sup> for a centrally-located, bilateral fin line. Figure 4.3.1 shows the computed values of cutoff frequency,  $f_c$ , the line impedance at infinite frequency,  $Z_{O\infty}$  and the effective dielectric constant,  $\epsilon_{eff}$ , as a function of gap width for several fin thicknesses near .012". The impedance at finite frequencies is given by

$$Z_O = \frac{Z_{O\infty}}{\sqrt{1 - (f_c/f)^2}}$$

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(9)

S. Hopfer, "The Design of Ridged Waveguides", MTT-3, 20, Oct 1955.

(10)

T. S. Chen, "Calculation of the Parameters of Ridge Waveguides", MTT-5, 12, Jan 1957.

(11)

J. R. Pyle, "The Cutoff Wavelength of the TE<sub>10</sub> Mode in Ridged Rectangular Waveguide of Any Aspect Ratio", MTT-14, 175, April '66.

(12)

A.M.K.Saad, G. Begemann, "Electrical Performance of Fin Lines of Various Configurations", Microwave, Optics, and Acoustics, MOA-1, 81, Jan 1977.

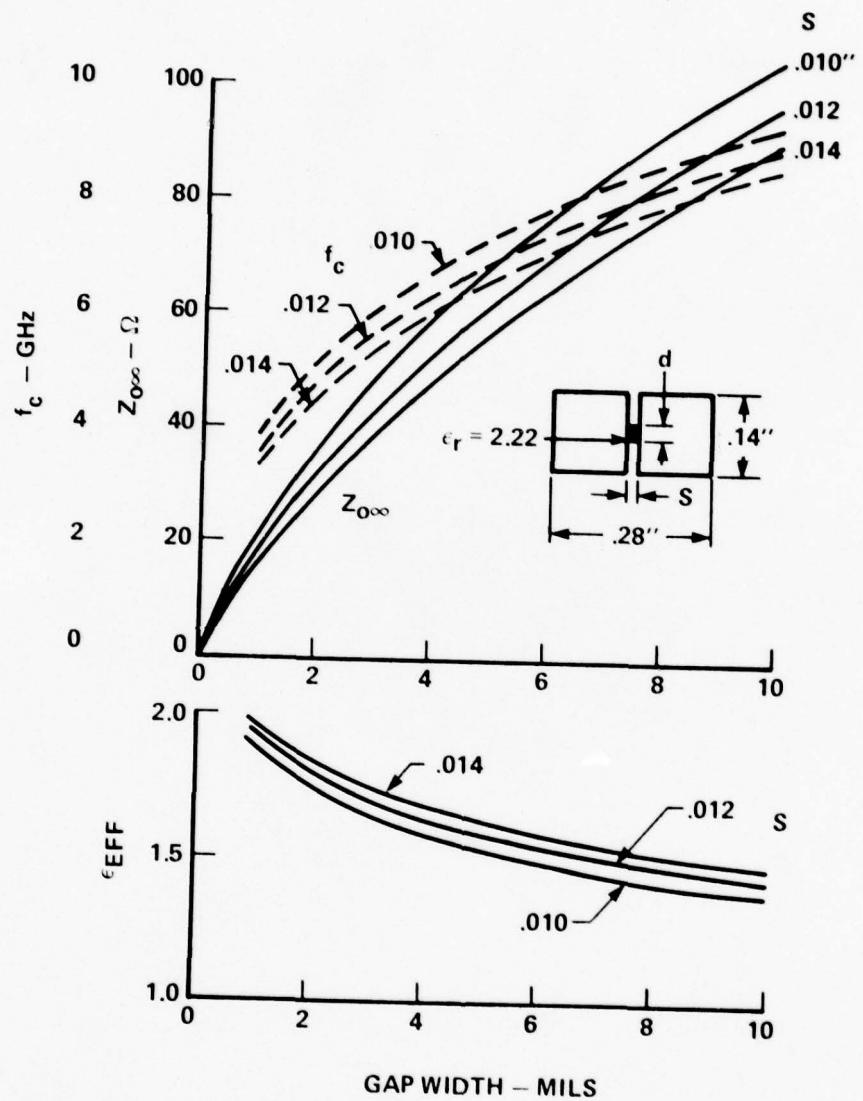


FIGURE 4.3.1. FINLINE PARAMETERS – DUROID IN WR-28 GUIDE

D-18928

The effective dielectric constant is given by

$$\epsilon_{\text{eff}} = (f_c'/f_c)^2$$

where  $f_c'$  is the cutoff frequency in the absence of the dielectric loading. Since it is defined at cutoff, it is independent of frequency and ignores the very slight dispersion due to the inhomogeneous dielectric. For our typical case with a .006" gap, .012" wide fin,  $f_c = 7.4 \text{ GHz}$ ,  $Z_{O\infty} = 70 \Omega$ ,  $\epsilon_{\text{eff}} = 1.55$ , and at 33 GHz  $Z_O = 58 \Omega$ . Thus, the (power-voltage) impedance is only moderately higher than in the microstrip case, so that we should not expect any serious limitations due to high line impedance.

#### 4.4 Switch Design

The principal features of the fin line switch design are sketched in Figure 4.4.1. The circuit with transitions and series slots is etched on both sides of a Duroid board with .010" dielectric thickness and .012" overall thickness. The PHS diodes are mounted on both sides of the board at the ends of the series slots, as indicated in Figure 4.1.1. The diode bond wires are .0007" gold, and we attempted to keep them as short as possible, without shorting out against the copper diode heat sinks. A short linear taper is cut in the Duroid in the full-height regions to match into the dielectric fins.

The board is clamped between two similar silver-plated housing blocks, containing the waveguide and choke channels. The waveguide height is reduced slightly in the tee junction to suppress a resonance which appeared with the fin line board in place in full-height guide.

The copper-clad areas on each side of the stem of the tee on the circuit board are insulated from the housing by 1-mil mylar tape, serving as the dc blocks. The area above the tee is not insulated and is the dc ground to the housing. The dc blocks add about 0.1 dB to the insertion loss.

The driver is situated in a cavity in the back of one of the blocks. The bias leads pass from the driver, through feed throughs in the block and make connection to the circuit board through holes cut in the mylar tape.

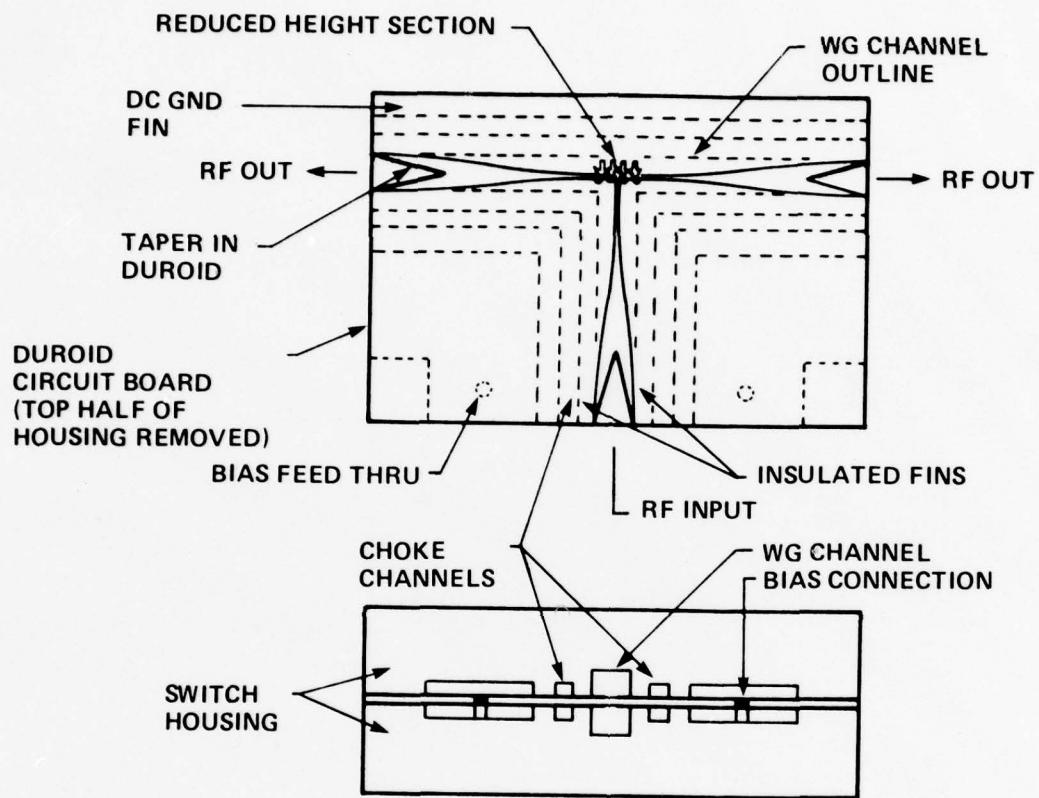


FIGURE 4.4.1. FINLINE SPDT CIRCUIT AND HOUSING LAYOUT

D-18942

The diode spacing was determined empirically as in the microstrip case. This will be discussed more fully in Section 5.1. The first diodes are located as close to the fin line tee-junction as practicable. The first bond wire is approximately .005" or 6 electrical degrees from the center line of the tee.

The complete switch is shown in Figure 4.4.2. Its overall size is 2.1 x 1.7 x 0.8", including the driver connector, and it weighs about 3 ounces. The housing was designed to accommodate the longer 1" taper transitions, although we used the 0.5" tapers in the final version. Therefore, the size could easily be reduced to 1.1 x 1.2 x 0.8", and its weight close to 1 ounce. The waveguide inputs are humidity sealed with teflon-fiberglass windows.



FIGURE 4.4.2. K<sub>A</sub>-BAND SPDT FINLINE SWITCH

D 18925

## 5.0 EXPERIMENTAL RESULTS - FINLINE

### 5.1 Finline Characteristics

In the course of developing the finline SPDT switch, we performed a series of experiments to examine some of the basic characteristics of finline. The preliminary measurements on insertion loss and match of a line with tapered transitions was covered in Section 4.2. The subsequent experiments involved various configurations of finline gaps and wires shunting the gaps, which can best be understood by reference to Figure 5.1.1.

In all cases the gaps were nominally .006" wide and .002" thick; the bond wires were .0007" dia. gold. In most cases the tapers were 1.0" long and the configuration was the same on both sides of the board. In the following, the term "a pair" of wires refers to the two wires on opposite sides of the board, at the same longitudinal position.

Figure 5.1.2 shows the isolation produced by one pair of straight wires shunting the gap and two pairs of wires with spacings of .065", .140" and .200". From the isolation of a single pair, curve 1, we deduce an inductance of approximately .046 nH, using 57.7 ohm for the line impedance at 33 GHz. We also ran a case with the wires arching over the gap, roughly doubling the wire length. This reduced the isolation by 1.5 dB, on the average, implying an inductance of .056 nH, only 22 percent greater than with short wires flat against the board. Similarly, the inductance of a single pair of .003" wide ribbons across the gap was .033 nH, and a single pair of "V" wires, as in Figure 5.1.1b, was approximately .024 nH.

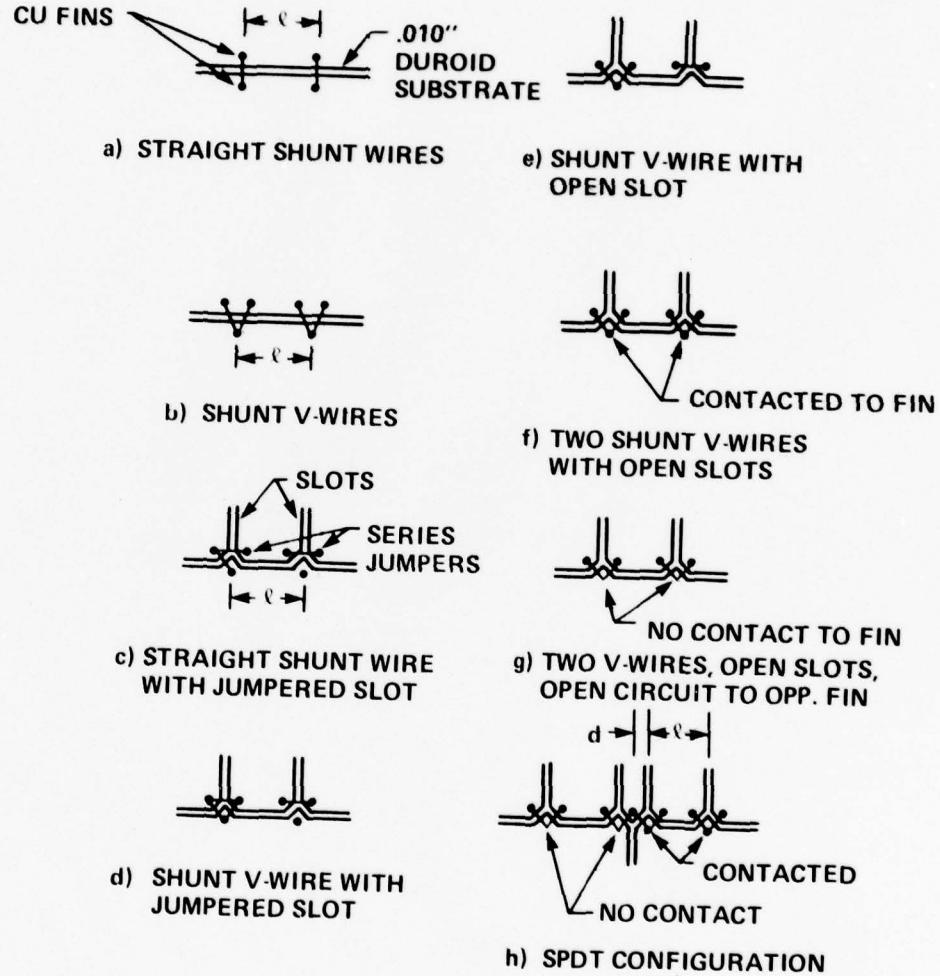


FIGURE 5.1.1. WIRE CONFIGURATIONS FOR FINLINE CIRCUIT TESTS

D-18943

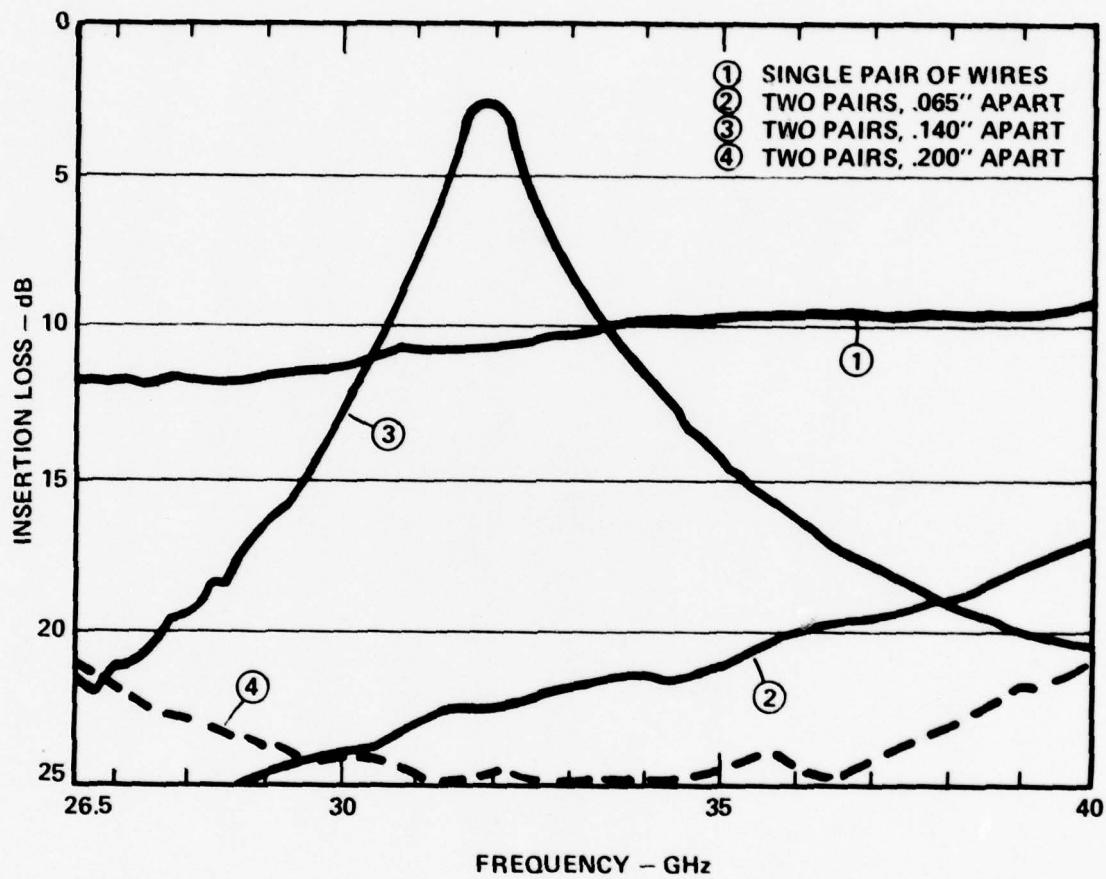


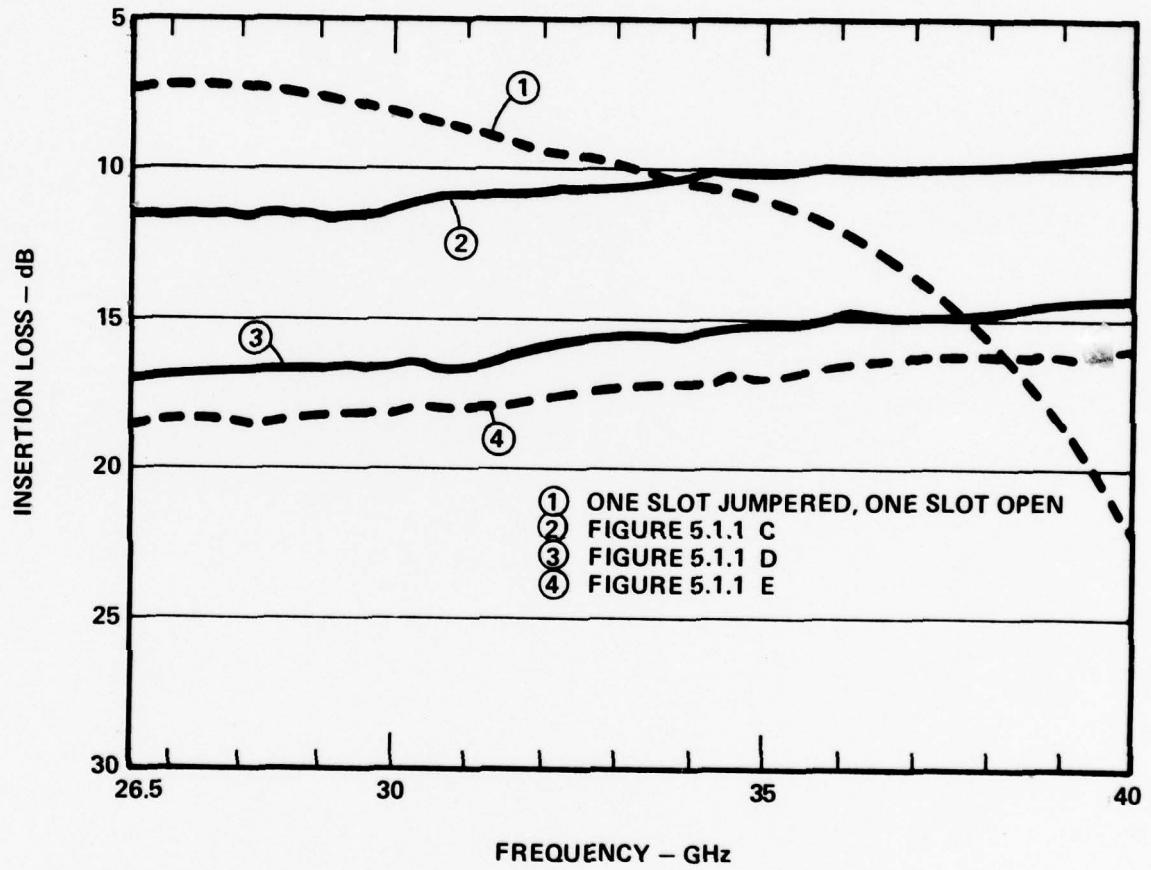
FIGURE 5.1.2. INSERTION LOSS OF .0007" WIRES SHUNTING A .006" FINLINE GAP

D-18930

The transmission resonance at 31.7 GHz, for two pairs of short wires spaced by .140", curve 3, implies a guide wavelength of .310", in good agreement with the value of .308" estimated from the computed cutoff frequency and effective dielectric constant, Figure 4.3.1.

Curve 3, is the isolation produced by two pairs of straight, short wires spaced .065" apart, which is approximately the theoretical optimum spacing for mid-band isolation. The isolation is 4-5 dB less than that calculated from the estimated inductance and the spacing. Curve 4 is the isolation for a spacing of .200", which is nominally  $3 \lambda_g/4$ . In this case, the maximum isolation, at mid-band is about 3 dB greater than for .065" spacing, and within 1.5 dB of the calculated value. These results indicate that the reason for less-than-expected isolation is the interaction of the higher-order evanescent modes of the closely spaced wires. Clearly the wide spacing improves the isolation, but at the expense of a much-reduced bandwidth.

Next, we did a series of measurements on a circuit which had a pair of slots perpendicular to the main fin line gap, as illustrated in Figures 5.1.1c-d. The slot spacing,  $\ell$ , was .066" and the gaps were .006". First we established that the loss and match of the circuit with both slots jumpered with wires, as shown on the right hand slot in Figure 5.1.1c were essentially the same as for the straight gap circuit. Figure 5.1.3 shows the results for the sequence shown in Figures 5.1.1c-d, and e. The isolation for a single shunt wire, with jumpered slots is the same as obtained in the straight gaps circuit as we would expect. Adding a second wire to form a V produces the isolation shown in curve 3,



**FIGURE 5.1.3. INSERTION LOSS OF SLOTTED FINLINE CIRCUIT FOR SEVERAL WIRE CONFIGURATIONS**

D-18934

which indicates that the inductance of the V-wires is .023 nH, about 2/3 that of the straight wires, agreeing with the results obtained on the unslotted circuit board. Opening up the series jumper wires between the legs of the V, Figure 5.1.1e, improves the isolation by approximately 1.5 dB. This improvement is far less than expected. We have calculated that the isolation should be over 30 dB in the lossless case, and 21-22 dB with as much as 3 ohms of series resistance (simulating a rather lossy diode). For the calculation, the slot was modeled as a parallel resonant circuit in series with the line between the legs of the V; the parameters were selected to produce a characteristic approximately matching the slot-only isolation in curve 1. The reason the slot is not as effective as calculated is not at all clear.

Next, in Figure 5.1.4, we have the characteristics of two pairs of V-wires simulating the responses with ideal, lossless, zero capacitance, diodes, Figures 5.1.1f and g. With the wires shunting the line, the isolation runs from about 30 to 23 dB, which is 12-14 dB less than we would expect from curve 4, Figure 5.1.3, due to the interaction of the closely spaced wires. With the apexes of the V's disconnected from the fin, to simulate the pass state of the switch, the insertion loss ran 0.5 to 0.9, and, except for the top end of the band, the match was better than 18 dB. Thus, the extra length of bond wire required to reach the diodes adds 0.2 - 0.3 dB of dissipative loss, and degrades the match somewhat, especially near 40 GHz. Figure 5.1.4 indicates that even with "ideal" diodes a fin line switch with two pairs of diodes will have much less isolation than a microstrip switch with two diodes, while the insertion loss and return loss in the pass state may be comparable or better.

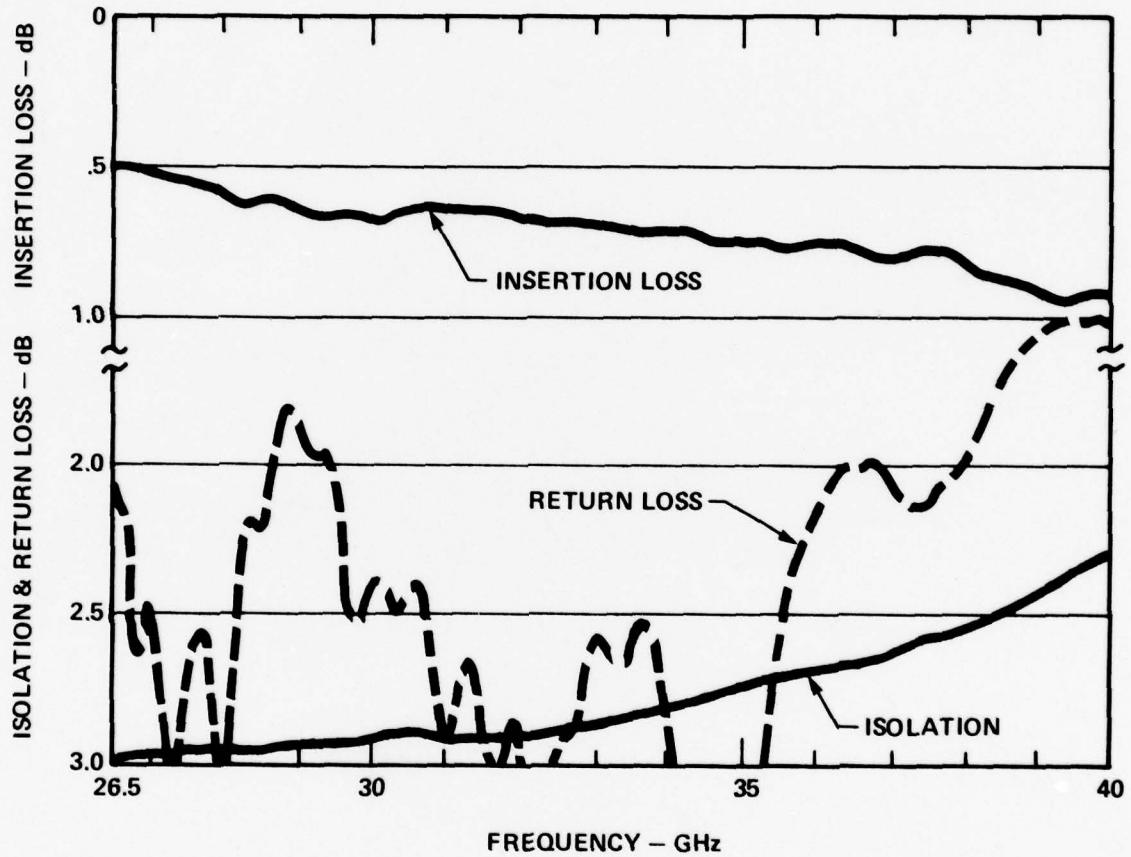


FIGURE 5.1.4. CHARACTERISTICS OF SPST SWITCH CIRCUIT WITH SHUNT V - WIRES OPEN AND SHORT CIRCUITED. "IDEAL DIODE" CASE.

D-18933

Figure 5.1.5 is the result with one pair of plated heat sink (PHS) diodes, corresponding to Figure 5.1.1e, but with real diodes. The isolation is approximately the same as obtained in the ideal case, Figure 5.1.3 curve 3, except that it is flatter due to the diode resistance.

In the pass state, however, the return loss is quite low and the insertion loss correspondingly high. The data imply a shunt capacitance value between .04 to .06 pF per diode, depending on how much additional inductance we allow for the bond wires, and how we model the slot. The estimated values for the diode capacitance is .02 - .03 pF, both from the manufacturer's specification and our measurements of reflection angle at K<sub>a</sub>-band with the diode terminating a 50 ohm microstrip line. Thus, in the fin line circuit, the effective capacitance of the diode is 2 to 3 times its value measured at low frequency or in a microstrip circuit.

As a consequence of the high shunt susceptance of the reverse-biased diodes, the insertion loss and match of the switch with two pairs of diodes is also rather high, as shown in Figure 5.1.6. Note that the best match occurs at the low end of the band, indicating that the diodes are too widely spaced to match up such large susceptances.

The isolation of the complete SPST switch in Figure 5.1.6 is in agreement with the simulated ideal case shown in Figure 5.1.4.

We also measured the characteristics of the SPDT switch with wires simulating ideal diodes as illustrated in Figure 5.1.1h. The diodes on one arm simulate forward biased diodes and on the other, reverse biased diodes. The results in Figure 5.1.7 show that the performance with respect to insertion

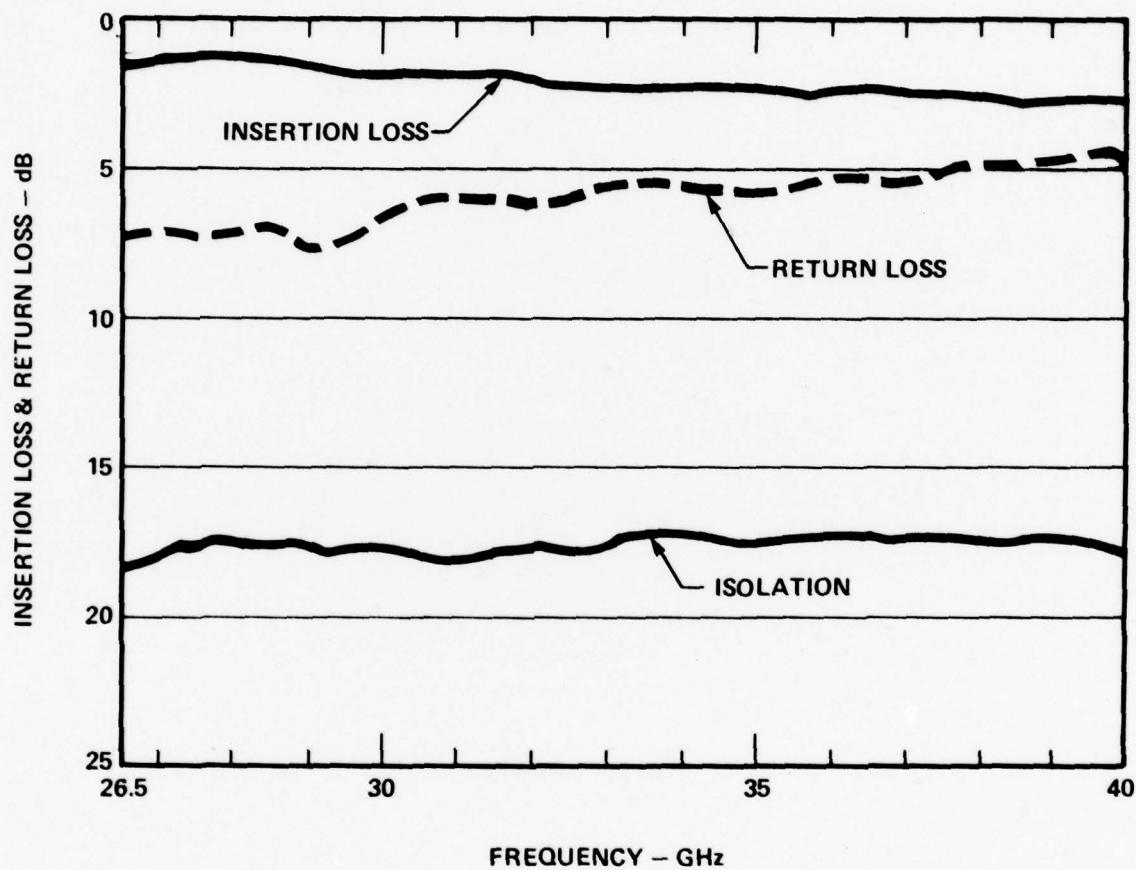


FIGURE 5.1.5 CHARACTERISTICS OF SPST SWITCH WITH ONE PAIR  
OF PHS DIODES

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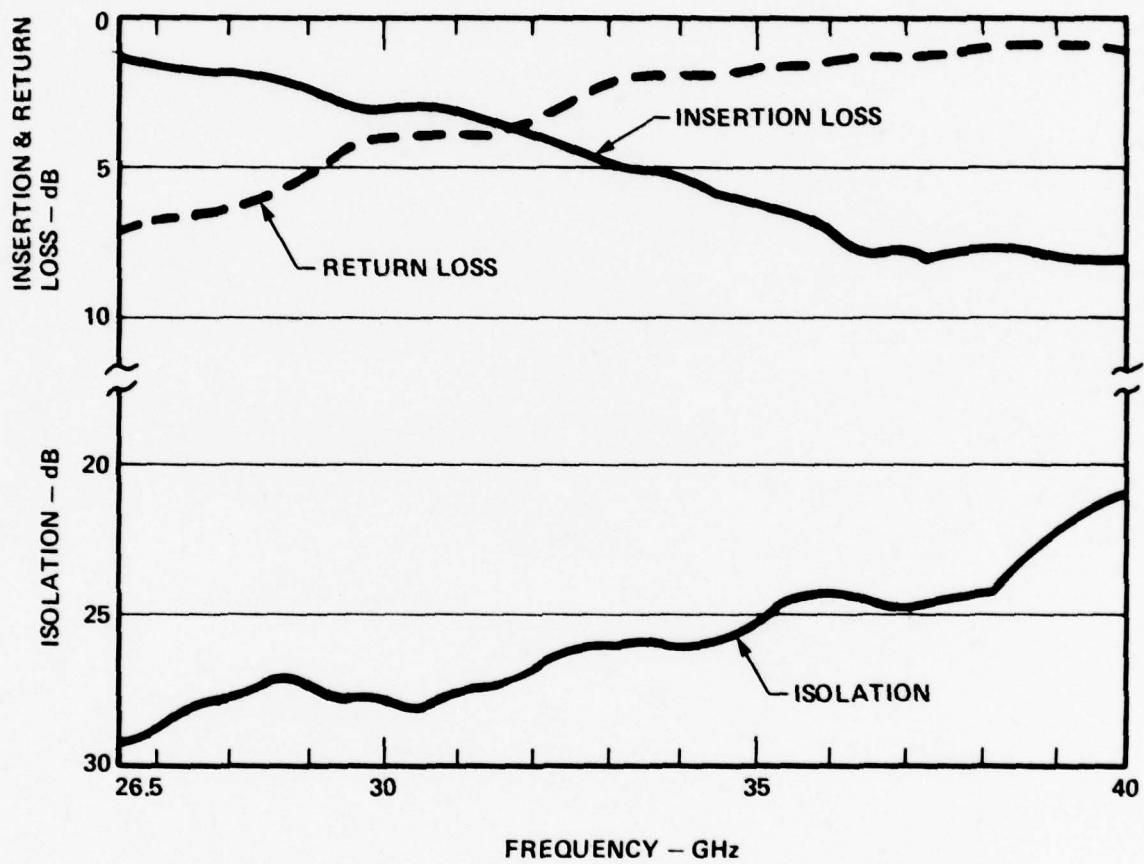


FIGURE 5.1.6. CHARACTERISTICS OF SPST SWITCH WITH 2 PAIRS  
OF PHS DIODES SPACED .066"

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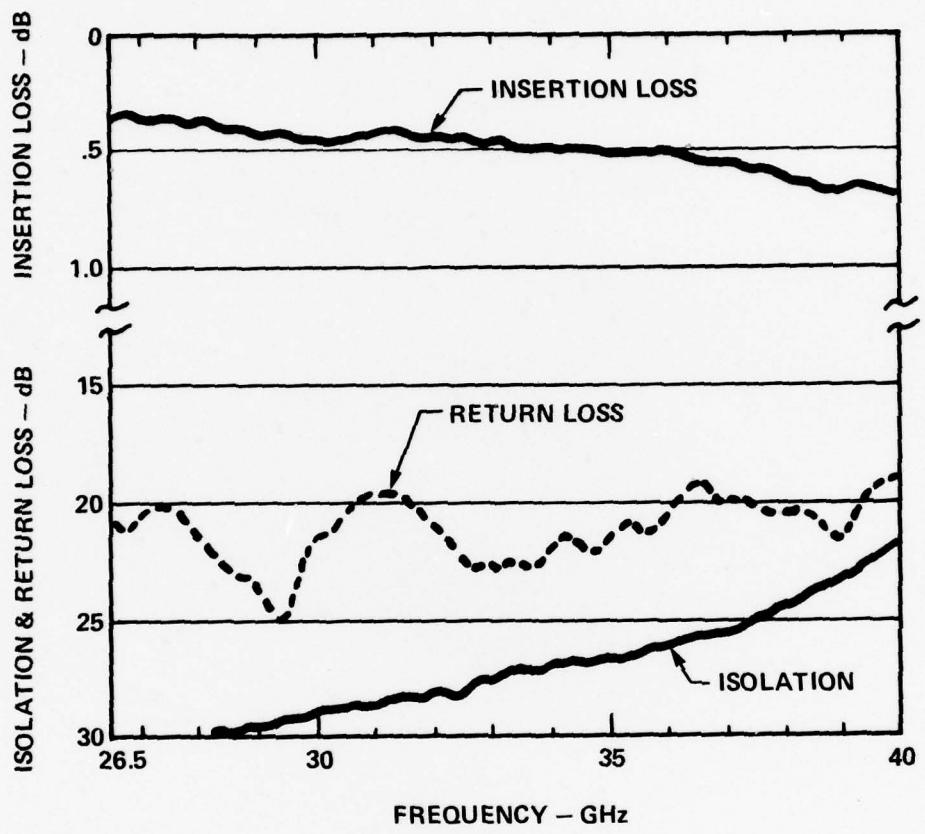


FIGURE 5.1.7. RESPONSES OF SPDT SWITCH CIRCUIT WITH SIMULATED  
"IDEAL DIODES". SHUNT WIRES AT JUNCTION AND  $\lambda/4$  AWAY

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loss, match, and isolation are slightly better than the corresponding SPST cases of Figure 5.1.4. It is not certain whether this better performance is inherent in the SPDT configuration, or is within the circuit-to-circuit variability we might expect, i.e. wire length and position, contact resistances, etc. Nevertheless, we expect that the performance with diodes will be comparable to that of the SPST switch.

Figure 5.1.8 shows the result of moving the pairs of shunt wires from the junction and  $\lambda/4$  away, to approximately  $\lambda/2$  and  $3\lambda/4$  away, moving them out of the center of the waveguide T-junction area, but maintaining the .066" spacing. There was a significant improvement in the isolation from 26.5 to about 36 GHz, but the bandwidth of the insertion loss side was markedly narrowed, as we should expect.

The experiments just described indicate first, that the isolation from the finline switch is significantly degraded due to the interaction of higher order modes, and second, that the insertion loss and mismatch in the pass state is much greater than can be accounted for on the basis of the individual component values. Nevertheless, much better in band insertion loss performance should be attainable by spacing the diodes more closely. Consequently we made new circuits for both the SPST and SPDT switch with the diode and series slot spacing reduced to .044". With these new circuits, we also used the shorter, 0.5" long, tapers.

Figure 5.1.9 shows the responses of the SPST circuit with wires corresponding to the "ideal diode" case, similar to Figure 5.1.4. In this case, however, we measured the responses with the non-contacting V wires very close (.001-.002") to the triangular points, i.e. "low" wires, and with them

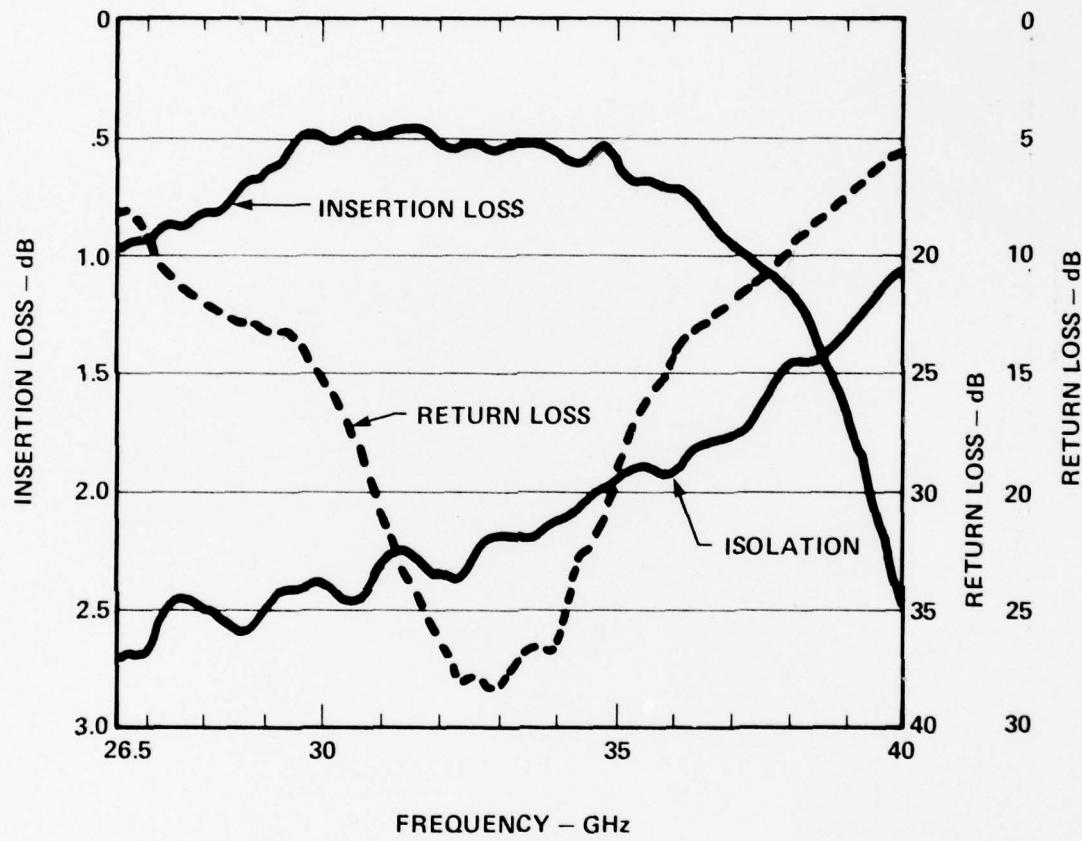


FIGURE 5.1.8. RESPONSES OF SPDT SWITCH CIRCUIT WITH SIMULATED  
"IDEAL DIODES". SHUNT WIRES AT  $\lambda/2$  AND  $3\lambda/4$  FROM JUNCTION

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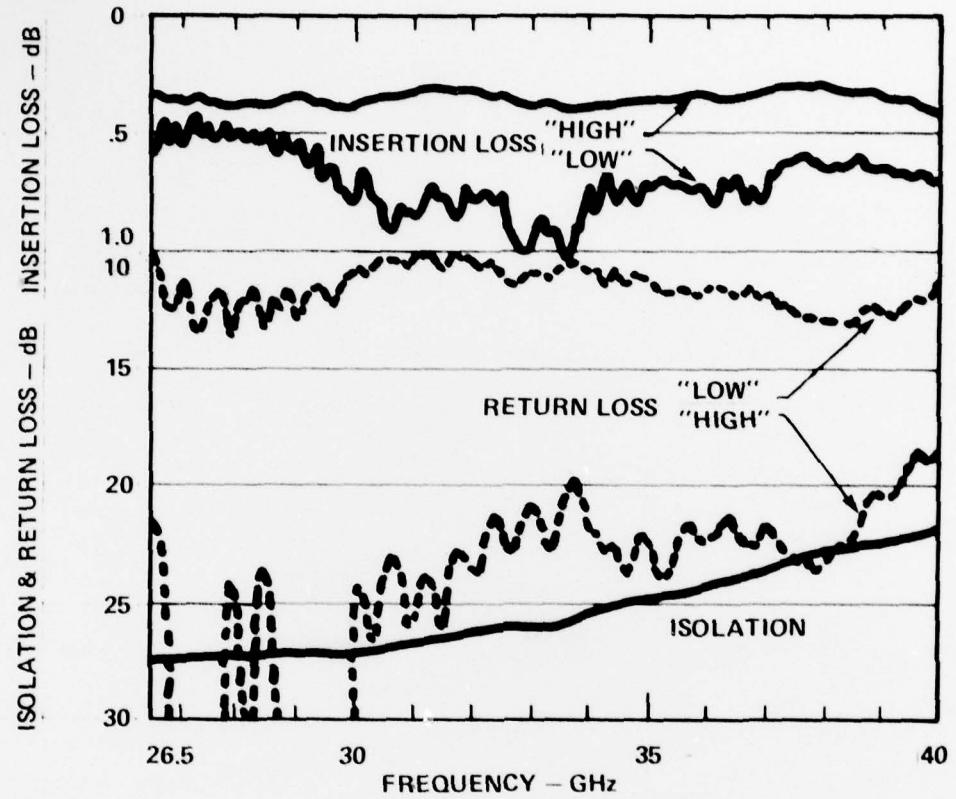


FIGURE 5.1.9. CHARACTERISTICS OF SPST SWITCH CIRCUIT WITH SHUNT V WIRES OPEN AND SHORT CIRCUITED AND .044" SPACING

D-18937

arched over the slots almost perpendicular to the board, i.e. "high" wires. Note that the "low" wires, although not adding very much, shunt capacitance--probably less than .01 pF--creates a substantial mismatch in this configuration.

The isolation produced by the .044" spaced wires is 2-3 dB less than that obtained with .066" spacing. This decrease is about what we would expect for the change in spacing, since it is no longer optimized for isolation; it need not be due to an increase in the interaction of higher order modes.

Figure 5.1.10 depicts the characteristics of this circuit as a full SPST switch with two pairs of PHS diodes. Clearly, moving the diodes closer together did move the best match frequency up close to midband, and the match remains reasonably good down to 26.5 GHz. However, the rolloff in return loss and insertion loss above mid band is quite rapid, such that the useful band is limited to below approximately 35 GHz.

Computer modeling of this response indicates that the effective capacitance is .08 - .12 pF (.04-.06 pF per diode), assuming that the wire inductance is in the 0.1 - .025 nH range. Since we do expect the inductance to be higher than in the "ideal diode" experiments, .05 nH is probably a reasonable estimate, in which case the effective capacitance is approximately .09 pF, or again about twice its expected value.

The isolation runs from 26 to 21 dB, about 1-2 dB less than with wires only. The change is comparable to that encountered in the .066" spacing measurements.

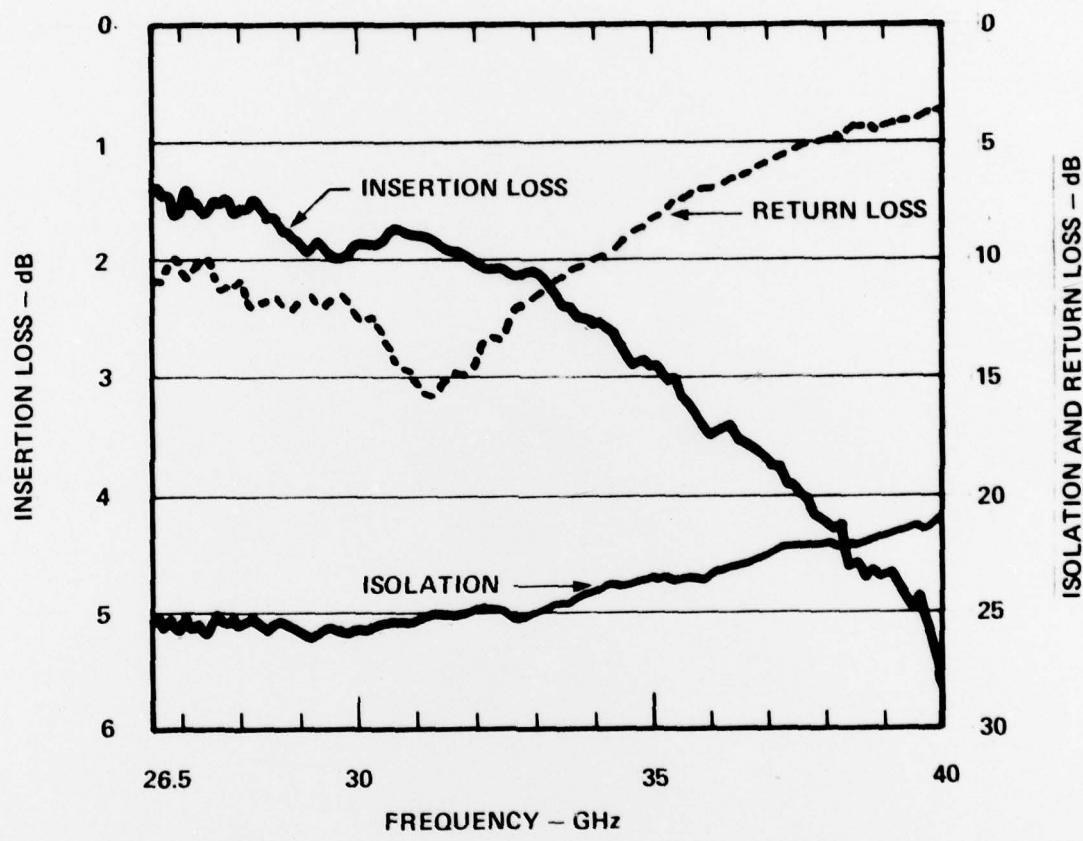


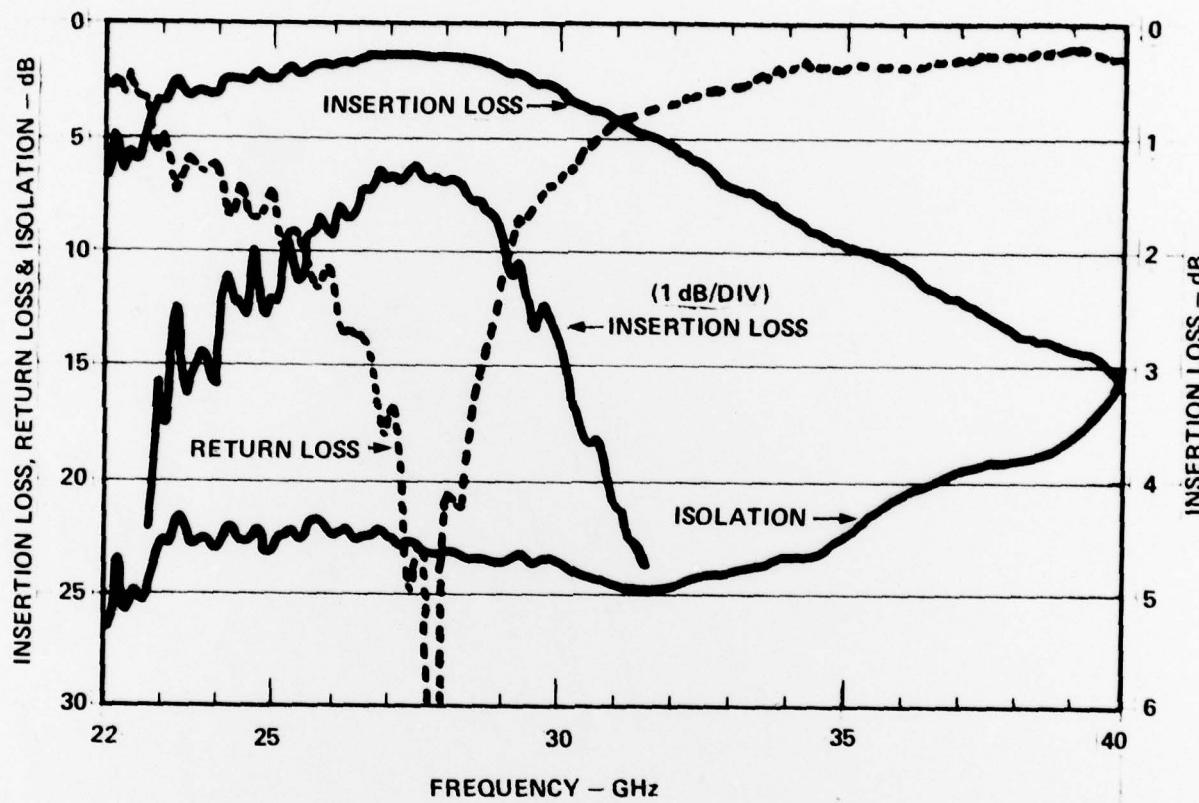
FIGURE 5.1.10. CHARACTERISTICS OF SPST SWITCH WITH TWO PAIRS OF P.H.S. DIODES SPACED .044"

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## 5.2 Switching Performance

Figures 5.2.1 and 5.2.2 show the switch performance in each state over the 22 to 40 GHz band. The performance of the double-throw switch corresponds, in general, to that of the single-throw switch shown in Figure 5.1.10. The insertion loss and return loss roll off markedly at the higher frequencies, severely limiting the useful bandwidth, and the isolation is only 20-25 dB within the passband.

In the J1-J3 direction, the passband insertion loss is flatter and lower than that of the SPST up to 32 GHz, but it drops off more rapidly above 35 GHz, while the return loss is somewhat lower. Note also that the passband cuts off rather sharply at about 23 GHz on the low side. The upper band edge of the passband in the J1-J2 direction is considerably lower. The reason for this is not entirely clear, since both arms of the switch look essentially the same. We had suspected that the length and dress of the wire bonds might be at fault, so, following the initial tests we made all the wires, on both arms, as short as possible, consistent with a 2-3 mil clearance above the diode ground plane. This did result in a significant improvement in the J1-J3 arm, moving the upper band edge up by about 2 GHz to its present state. It had a negligible effect on the J1-J2 arm. Our modeling experiments suggest that the effective capacitance is high. This could come about if the wire bond to one diode creates excessive fringing capacitance where the compressed area of the wire overhangs the 1-mil dot on the diode. Since the overall performance of the finline switch was not as good as the microstrip switch, and our supply of PHS diodes exhausted, we did not attempt to improve the J1-J2 arm to equal the J1-J3 side.



**FIGURE 5.2.1 TRANSMISSION RESPONSES OF FINLINE SPDT SWITCH, J1-J2  
REFLECTION RESPONSE CORRESPONDING TO INSERTION  
LOSS CASE**

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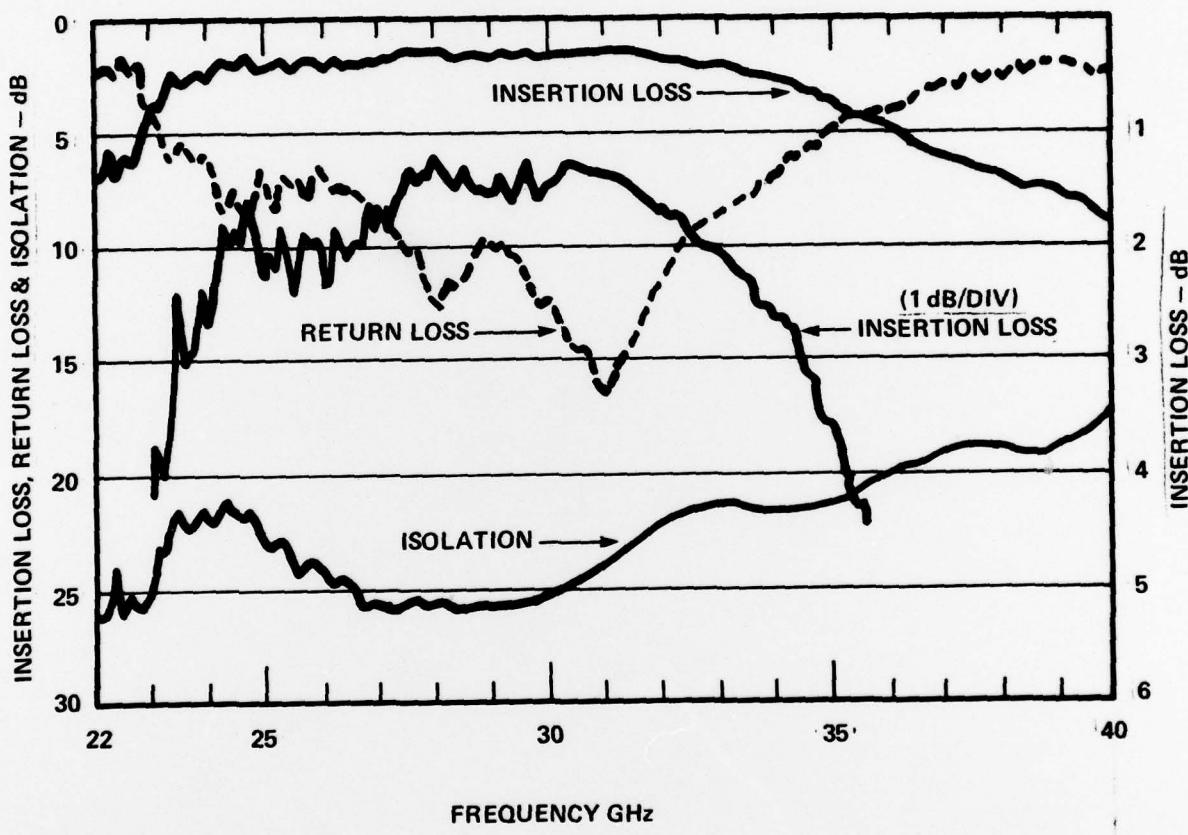


FIGURE 5.2.2. TRANSMISSION RESPONSES OF FINLINE SPDT SWITCH, J1-J3  
REFLECTION RESPONSE CORRESPONDING TO INSERTION  
LOSS CASE

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Within the passbands, where the reflection loss is negligible, the insertion loss is approximately 1.3 dB. This is comparable to the loss of the microstrip switch, but it is clearly not an improvement over the latter.

Because the narrow bandwidth of this switch is probably due to the high effective capacitance of the diodes, we measured the responses with diodes on only one side of the board. In constructing the final switch, we first drilled .014" holes through the board where each diode and bond wire would be located, and contacted the two sides by filling the holes with solder. The diodes were installed on one side only and the characteristics measured from 22 to 40 GHz.

First, the isolation in the passband was nominally 14 dB, J1-J2, and 17 dB, J1-J3. The passbands were somewhat wider--J1-J2 cut off at about 33 GHz and J1-J3 at about 36 GHz. The match in the passbands was not as good as with all eight diodes, although we made no attempt to improve it with tuning. The low frequency cutoff was at 23 GHz for both directions. Although the bandwidth was slightly wider with only one set of diodes, since the band did not extend to 40 GHz, we felt the improvement did not outweigh the reduction in isolation. Therefore, we did not pursue this asymmetrical approach further.

The switching speed characteristics of the completed SPDT fin line switch was the same as those of the microstrip switch, as described in Section 3.1 and Figure 3.1.3.

### 5.3 Discussion

It is clear that the finline SPDT switch performance is inferior to that of the microstrip switch. Its principal shortcomings are in the relatively low isolation produced and in the narrow bandwidth of the pass state.

Interestingly, the low isolation was less due to the series inductance, as we had expected, but more to the interaction of the evanescent modes around the closely spaced diodes. The reason for the narrow pass state bandwidth is less clear cut. However, the experiments and modeling calculations strongly suggest that it arises from excess fringing capacitance of the wire bond on top of the diode and of the wires passing over the metal fin to reach the diode. Clearly, excess capacitance generated this way would be a direct consequence of the chip and wire bond technique.

Hofmann, et al,<sup>(3)</sup> reported results on a two-throw K<sub>A</sub>-band finline switch using beam lead PIN diodes. They did not report any design details, but its insertion loss was just over 1 dB and the isolation was 20-21 dB from 26.5 to 35 GHz. The insertion loss gently increased to about 2.5 dB and the isolation decreased to 17 dB at 40 GHz. Note that, aside from the severe high frequency rolloff on our circuit, the performances of the two switches are quite comparable. Thus, we would attribute the narrow bandwidth we obtained to the use of the chip-and-wire-bond construction.

#### 6.0 CONCLUSIONS AND RECOMMENDATIONS

The K<sub>a</sub>-band microstrip SPDT switch developed on this program met all of the design requirements set forth on page 1. Also, it met or exceeded the design goals for insertion loss and isolation from 26.5 to 34 GHz, for amplitude tracking over the entire K<sub>a</sub>-band, and for the RF transition speed. As experience is gained in building future units, we expect to improve the insertion loss and isolation above 34 GHz to 2.1 dB max. and 40 dB min., respectively.

The plated heat sink diodes, with their low capacitance, high Q, and thin I-layers, are superbly suited to this high speed, millimeter wave switch application. They were the key to the switch performance attained on this program.

The switch will readily handle 2.5 watts of CW power with, at most, a slight (< 1 dB) decrease in isolation above 1.8 watts. We believe that with higher bias current, 40-50 mA, acceptable performance will be achieved in the 3 to 4 watt range.

There are three particular areas in which future development work on this switch should be undertaken.

The first is to ascertain the causes for the high frequency rolloffs in insertion loss and isolation. Elimination or reduction of these effects will result in a K<sub>a</sub>-band switch with performance comparable to X-band switches using conventional diodes.

Second is to broadband the switch to cover the 18-40 GHz frequency range. This involves two separate aspects, the microstrip circuit and the transitions. The circuit work would be addressed to improving the diode mountings to reduce the series inductance, and to adding a broadbanding transformer in the T-junction. The broadband

microstrip portion alone would then be suitable for integrated circuit package, since transitions to waveguide would not be necessary.

The design of a broadband launcher will depend, of course, on the type of feed guide to be used. A broadband waveguide feed would no doubt be either single or double ridge guide; the design of new tapers to a ridge guide microstrip launcher should be relatively straightforward.

The third area is to look at additional methods to reduce production costs. The waveguide-microstrip transition deserves particular consideration in this respect. A transition, etched on the same circuit board as the microstrip line, as illustrated in Figure 6.0.1, has been developed at NOSC.\* Such a transition would not only reduce materials costs and labor costs, since no manual tuning would be required, it would also result in a much smaller, more compact package.

The performance of the finline switch fell far short of the design goals and requirements. The pass state passband was quite narrow and the isolation was relatively low over the entire  $K_A$ -band. We concluded that the insertion loss bandwidth problem was attributable to excess fringing capacitance associated with the diode bond wires. The low isolation was due to the interaction of higher order, evanescent, modes around the diodes.

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\* D. Rubin, D. Saul, Naval Ocean Systems Center, San Diego, CA, private communication.

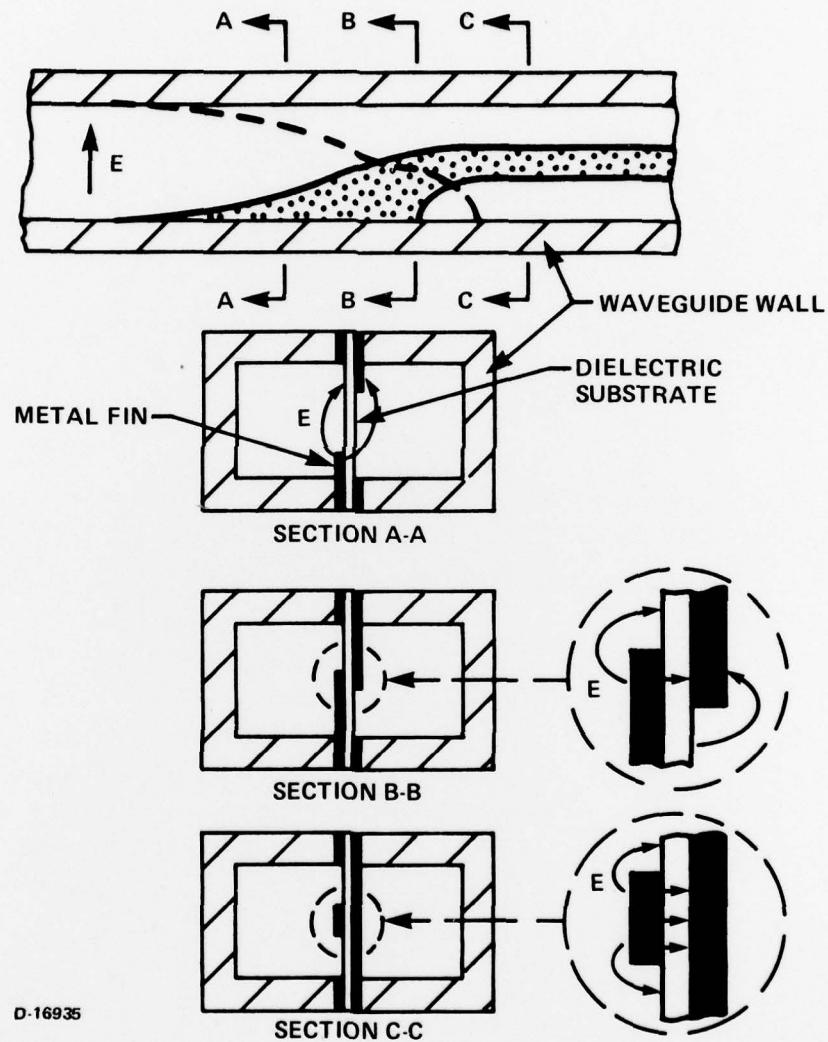


FIGURE 6.0.1 WAVEGUIDE-MICROSTRIP TRANSITION

A finline switch using beam lead diodes, reported by Hofmann<sup>(3)</sup>, had full bandwidth, but its isolation was comparable to ours, also because of the evanescent mode interaction. One could improve the mid band isolation by going to  $3\lambda/4$  diode spacing, but the bandwidth in both states would shrink appreciably.

Thus, at best, a finline switch will not have the isolation performance readily attainable in a microstrip switch. Furthermore, any insertion loss advantage of a finline switch appears to be quite marginal. We believe that improvements in the microstrip switch, such as the printed circuit transition, could erase the advantage entirely.

We conclude that the chip-and-wire-bond construction technique is totally unsuitable for finline switches. Also, even with beam lead diodes, a finline switch is inferior to microstrip and that further development would best be applied to the microstrip configuration.

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The report describes the plated heat sink PIN diodes and the waveguide to microstrip and finline transitions used in the designs. Final performance data are presented and compared for both types of switches. Concludes that microstrip is the superior medium for integrated circuit switches.

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